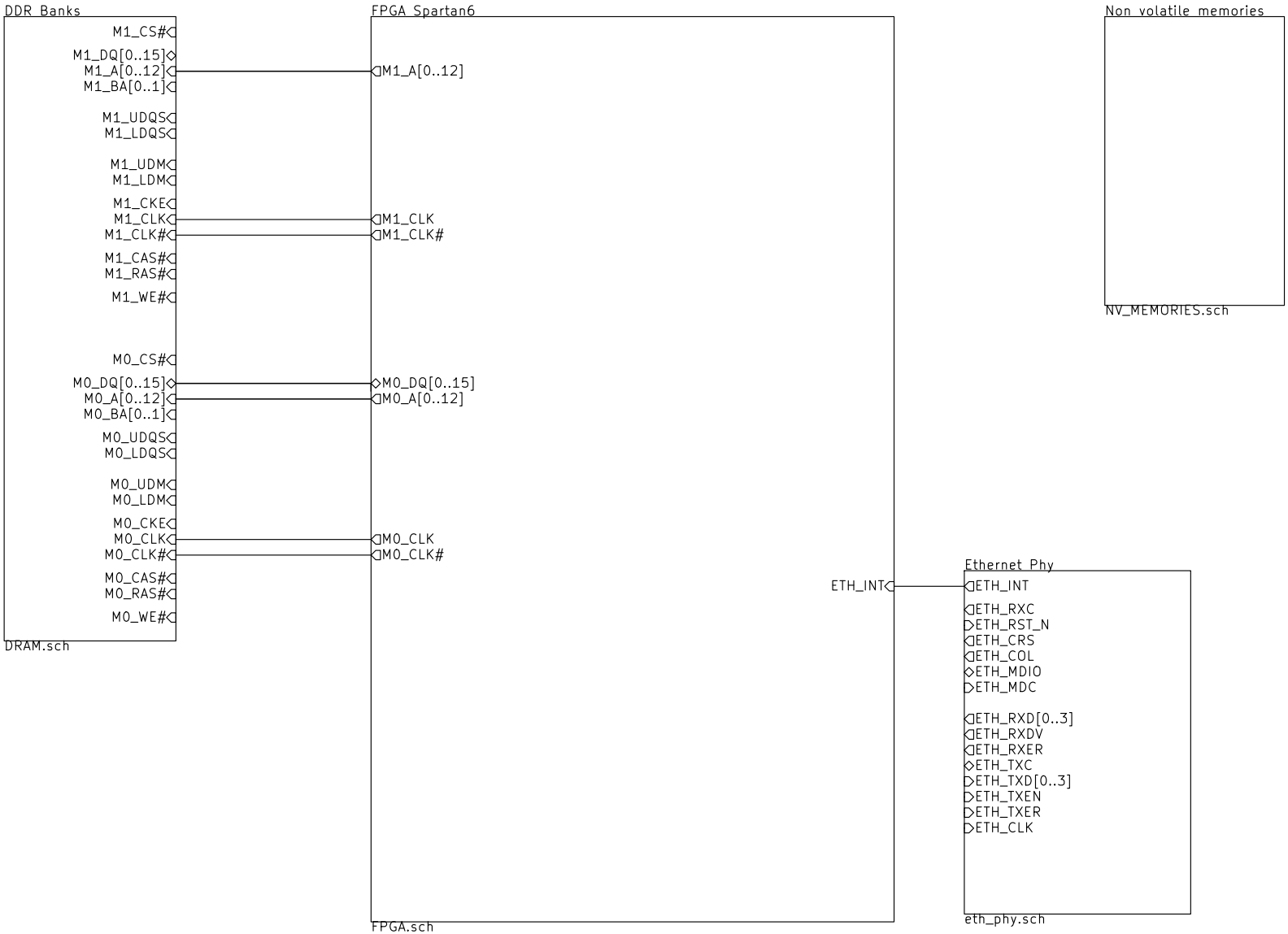
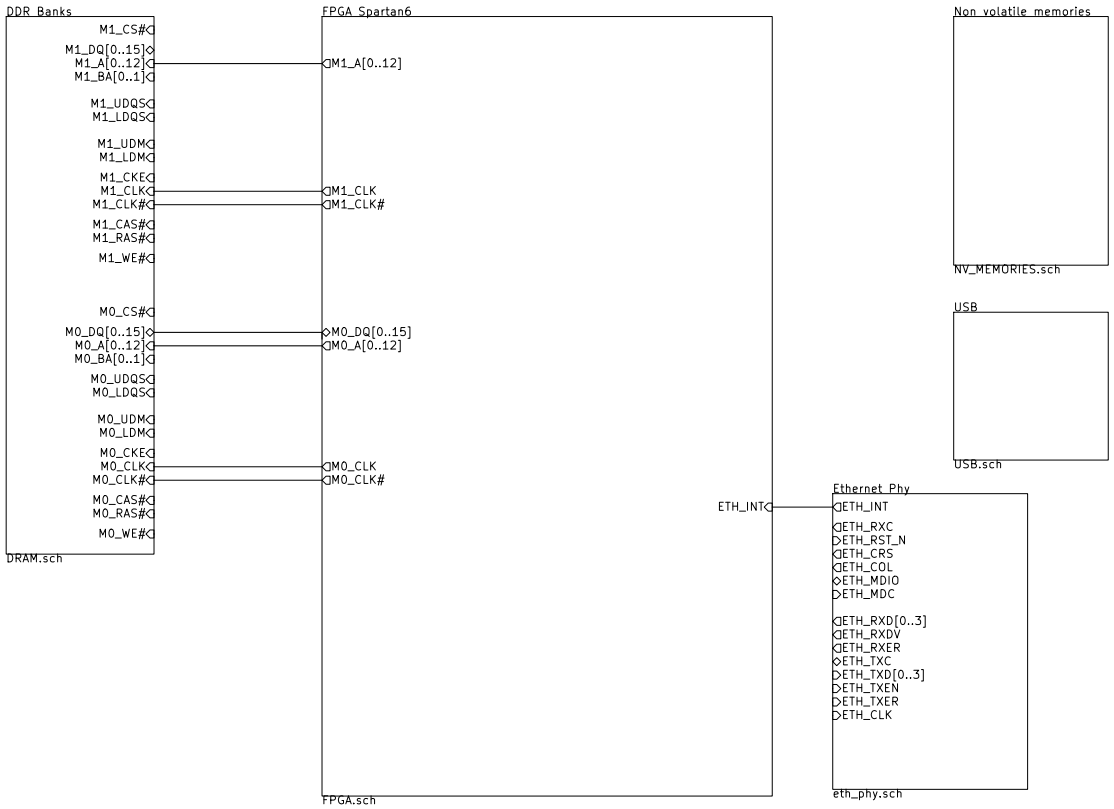

DDR Banks
M1_CS#
M1_DQ[0..15]
M1_A[0..12]
M1_BA[0..1]
M1_UDQS
M1_LDQS
M1_UDM
M1_LDM
M1_CKE
M1_CLK
M1_CLK#
M1_CAS#
M1_RAS#
M1_WE#
M0_CS#
M0_DQ[0..15]
M0_A[0..12]
M0_BA[0..1]
M0_UDQS
M0_LDQS
M0_UDM
M0_LDM
M0_CKE
M0_CLK
M0_CLK#
M0_CAS#
M0_RAS#
M0_WE#
DRAM.sch
FPGA Spartan6
M1_A[0..12]
M1_CLK
M1_CLK#
M0_DQ[0..15]
M0_A[0..12]
M0_CLK
M0_CLK#
ETH_INT
FPGA.sch
Non volatile memories
NV_MEMORIES.sch
Ethernet Phy
ETH_INT
ETH_RXC
ETH_RST_N
ETH_CRS
ETH_COL
ETH_MDIO
ETH_MDC
ETH_RXD[0..3]
ETH_RXDV
ETH_RXER
ETH_TXC
ETH_TXD[0..3]
ETH_TXEN
ETH_TXER
ETH_CLK
eth_phy.sch


DDR Banks
M1_CS#
M1_DQ[0..15]
M1_A[0..12]
M1_BA[0..1]
M1_UDQS
M1_LDQS
M1_UDM
M1_LDM
M1_CKE
M1_CLK
M1_CLK#
M1_CAS#
M1_RAS#
M1_WE#
M0_CS#
M0_DQ[0..15]
M0_A[0..12]
M0_BA[0..1]
M0_UDQS
M0_LDQS
M0_UDM
M0_LDM
M0_CKE
M0_CLK
M0_CLK#
M0_CAS#
M0_RAS#
M0_WE#
DRAM.sch
FPGA Spartan6
M1_A[0..12]
M1_CLK
M1_CLK#
M0_DQ[0..15]
M0_A[0..12]
M0_CLK
M0_CLK#
ETH_INT
FPGA.sch
Non volatile memories
NV_MEMORIES.sch
USB
USB.sch
Ethernet Phy
ETH_INT
ETH_RXC
ETH_RST_N
ETH_CRS
ETH_COL
ETH_MDIO
ETH_MDC
ETH_RXD[0..3]
ETH_RXDV
ETH_RXER
ETH_TXC
ETH_TXD[0..3]
ETH_TXEN
ETH_TXER
ETH_CLK
eth_phy.sch