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# Purpose and Scope

The purpose of this document is to capture validation and verification requirements for General Purpose Baseband Computing (GBC) module as part of Open Cellular Base Transceiver Station (BTS). The document is intended to provide fundamental set of test specifications required to ensure consistent and reliable operation of GBC in a BTS system under all supported operating and environmental conditions.

These test specifications cover following subsystems of GBC:

* + Front Panel Sub-system
  + Power Sub-System
  + CPU Sub-system
  + TIVA Sub-system
  + Ethernet Sub-system
  + Clock Sub-system

# Abbreviation

GBC General Purpose Baseband Controller

PoE Power over Ethernet

PD Powered device

PSE Power Sourcing Equipment

EV Electrical Validation

SI Signal Integrity

FV Functional Validation

RF-SDR Radio frequency Software-Defined Radio\

BTS Base Transceiver Station

# Front Panel Sub-system

The Front Panel Sub-System constitutes of power input section. There are three input power sources for GBC board- Solar panel input, Auxiliary supply and PoE.

## Test Purpose and Description

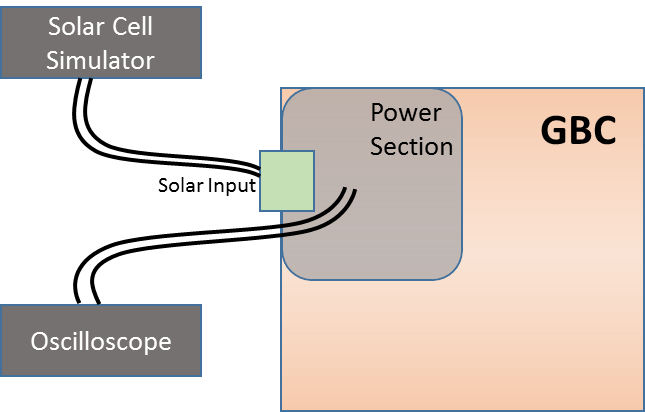
The purpose of this test is to ensure the accuracy and range of all the supply inputs with which GBC can be powered.

## Front Panel Sub-system constitutes of below components

1. Solar supply input
2. AUX supply input
3. PoE input
4. PSE out
5. Protection

### Solar Supply Input

#### Test Setup



**Figure 1. Solar Supply Input - Test Setup Diagram**

#### Test Case: Voltage Accuracy (Test ID: FP.1.1)

##### **Description**

1. **Purpose**

Solar power input is designed to work in the range of 16 to 22V. The purpose of the test case is to ensure the accuracy of the solar supply voltage is as per the designed margins.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | GBC will not be powered up if PoE and/or Batteries are absent. |
| Performance | Yes |  |
| Compliance | NA | NA |

**Table 1. Impact of Failure – Solar Voltage Accuracy**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| VPSOLAR | JTB10A.1 |
| VSLR\_OVUVOUT | R1304.2 |
| VSLRPOE\_VOUT | C3M171.1 |
| VPS\_VOUT | C1685.1 |

**Table 2. Measurement Locations – Solar Voltage Accuracy**

##### **Test Equipment List**

1. Solar cell array simulator: Agilent E4350B

2. Digital Oscilloscope: MSO9404A

##### **Equipment Settings**

1. Solar cell array simulator: Configure the equipment in Array Simulator mode
2. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50ms

Bandwidth: 20MHz

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

1. Keysight Command Expert

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 3. Test Condition – Solar Voltage Accuracy**

##### **DUT Settings**

1. Isolated input side of Tiva controller by removing the resistor R10054.
2. Isolated input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Measurement Parameter** | **JTB10A.1** | **R1304.2** | **C3M171.1** | **C1685.1** |
| Input Voltage(V) | 16 to 22 | 16 to 22 | 16 to 22 | 16 to 22 |

**Table 4. Requirements – Solar Voltage Accuracy**

##### **Test Procedure**

1. Remove resistor R10067 and R10054 in order to isolate Intel processor and TIVA respectively.
2. Configure Solar Cell simulator to simulate a solar voltage of 18V
3. Measure the voltage at R1304.2 and make sure the voltage is 18V+/- 5%.

##### **Reference**

Further details can be found in Page 40, 48 and 53 of GBC schematic Ver. Life-2.

#### Test Case: Input Voltage Range (Test ID: FP.1.2)

##### **Description**

1. **Purpose**Solar power input is designed to work in the range of 16 to 22V. The purpose of the test case is to validate the range of solar input voltages for which GBC will be functional.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | GBC will not be powered up if PoE and/or Batteries are absent or Aux/Solar power is less than 16.27V |
| Performance | Yes |  |
| Compliance | NA | NA |

**Table 5. Impact of Failure – Solar Input Voltage Range**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| VPSOLAR | JTB10A.1 |
| VSLR\_OVUVOUT | R1304.2 |
| VSLRPOE\_VOUT | C3M171.1 |
| 12V\_IN | R10044.2 |

**Table 6. Measurement Locations – Solar Input Voltage Range**

##### **Test Equipment List**

1. Solar cell array simulator: Agilent E4350B

2. Digital Oscilloscope: MSO9404A

##### **Equipment Settings**

1. Solar cell array simulator: Configure the equipment in Array Simulator mode
2. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50ms

Bandwidth: 20MHz

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

1. Keysight Command Expert

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table7. Test Condition – Solar Input Voltage Range**

##### **DUT Settings**

1. Isolated input side of Tiva controller by removing the resistor R10054.
2. Isolated input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Measurement Parameter** | **JTB10A.1** | **R1304.2** | **C3M171.1** | **R10044.2** |
| Voltage(V) | 16 to 22 | 16 to 22 | 16 to 22 | 12 |

**Table 8. Requirements – Solar Input Voltage Range**

##### **Test Procedure**

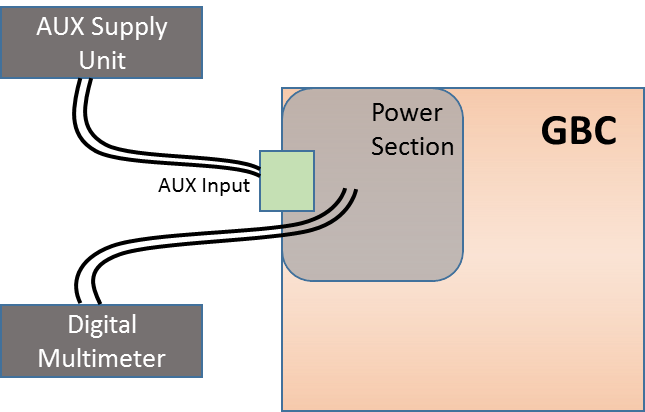
1. Remove resistor R10067 and R10054 in order to isolate Intel processor and TIVA respectively.
2. Configure Solar Cell simulator to give a voltage in the range of 16V to 22V
3. Varying the simulator for voltages in steps of 2V, measure the input voltage at JTB10A.1, R1304.2 and C3M171.1 and make sure the voltages are in the range of 16V to 22V
4. For every step of solar input voltage, measure the output voltage of Buck-Boost converter (U88) at R10044.2.
5. The Buck-Boost output should be 12V to ensure proper functionality of GBC module

##### **Reference**

Further details can be found in Page 40, 48 and 53 of GBC schematic Ver. Life-2

### Auxiliary Supply input

#### Test Setup



**Figure 2. Auxiliary Supply Input - Test Setup Diagram**

#### Test Case: Voltage Accuracy (Test ID: FP.2.1)

##### **Description**

1. **Purpose**

AUX power supply input is designed to work with the voltage in range of 16V to 24V. The purpose of this test case is to validate the input voltage accuracy of AUX input voltage.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | GBC will not be powered up if PoE and/or Batteries are absent. |
| Performance | NA |  |
| Compliance | NA | NA |

**Table 9. Impact of Failure – auxiliary Voltage Accuracy**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| VPSOLAR | JTB10A.1 |
| VSLR\_OVUVOUT | R1304.2 |
| VPS\_VOUT | C1685.1 |
| VSLRPOE\_VOUT | C3M171.1 |

**Table 10. Measurement Locations – auxiliary Voltage Accuracy**

##### **Test Equipment List**

1. AUX Power supply unit: Agilent E3634A
2. Oscilloscope: MSO9404A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 24V

Current Limit: 1.5A

OVP: 26V

OCP: 2A

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50ms

Bandwidth: 20MHz

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 16V - 24V | Nominal input voltage range |
| Temperature | +25 C | Normal Room temperature |

**Table 11. Test Condition – auxiliary Voltage Accuracy**

##### **DUT Settings**

1. Isolated input side of Tiva controller by removing the resistor R10054.
2. Isolated input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Measurement Parameter** | **JTB10A.1** | **R1304.2** | **C3M171.1** | **C1685.1** |
| Input Voltage(V) | 16 - 24 | 16 - 24 | 16 - 24 | 16 - 24 |

**Table 12. Requirements – Auxiliary Voltage Accuracy**

##### **Test Procedure**

1. Remove resistor R10067 and R10054 in order to isolate Intel processor and TIVA respectively.
2. Configure AUX power supply to give a voltage in range of 16V to 24V.
3. Measure the input voltage at JTB10A.1, R1304.2, C3M171.1, and C1685.1.
4. The above measured voltage should be equal to the set voltages of AUX power supply unit to ensure proper functionality of GBC module.

##### **Reference**

Further details can be found in Page 40, 48 and 53 of GBC schematic Ver. Life-2.

#### Test Case: Input Voltage Range (Test ID: FP.2.2)

##### **Description**

1. **Purpose**

AUX power supply input is designed to work in the range of 16 to 24V. The purpose of the test case is to validate the range of AUX input voltages for which GBC will be functional.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | GBC will not be powered up if PoE and/or Batteries are absent and Aux/Solar power is less than 16.27V |
| Performance | NA |  |
| Compliance | NA | NA |

**Table 13. Impact of Failure – Auxiliary Input Voltage Range**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| VPSOLAR | JTB10A.1 |
| VSLR\_OVUVOUT | R1304.2 |
| VSLRPOE\_VOUT | C3M171.1 |
| 12V\_IN | R10044.2 |

**Table 14. Measurement Locations – auxiliary Input Voltage Range**

##### **Test Equipment List**

1. AUX Power supply unit: Agilent E3634A

2. Digital Oscilloscope: MSO9404A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 24V

Current Limit: 1.5A

OVP: 26V

OCP: 2A

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50ms

Bandwidth: 20MHz

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 15. Test Condition – auxiliary Input Voltage Range**

##### **DUT Settings**

1. Isolated input side of Tiva controller by removing the resistor R10054.
2. Isolated input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Measurement Parameter** | **JTB10A.1** | **R1304.2** | **C3M171.1** | **R10044.2** |
| Voltage(V) | 16 to 24 | 16 to 24 | 16 to 24 | 12 |

**Table 16. Requirements – auxiliary Input Voltage Range**

##### **Test Procedure**

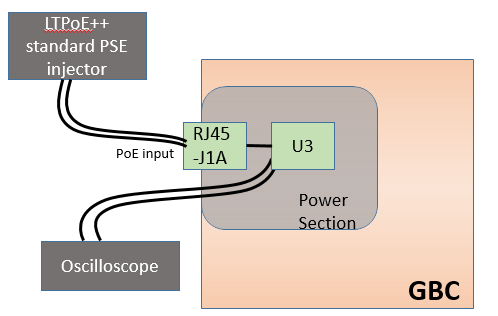
1. Remove resistor R10067 and R10054 in order to isolate Intel processor and TIVA respectively.
2. Configure AUX power supply to give a voltage in the range of 16V to 24V
3. Varying the AUX supply for voltages in steps of 2V, measure the input voltage at JTB10A.1, R1304.2, C3M171.1, and make sure the voltages are in the range of 16V to 24V.
4. For every step of AUX input voltage, measure the output voltage of Buck-Boost converter (U88) at R10044.2.
5. The Buck-Boost output should be 12V to ensure proper functionality of GBC module.

##### **Reference**

Further details can be found in Page 40, 48 and 53 of GBC schematic Ver. Life-2

### PoE IN

#### Test Setup



**Figure 3. PoE IN - Test Setup Diagram**

#### Test Case: Voltage accuracy (Test ID: FP.3.1)

##### **Description**

1. **Purpose**

The purpose of this test case is to check the voltage accuracy of input side voltage rails when GBC is powered through PoE.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | If input voltage is less than or more than the designed limit, the powering on of GBC will be affected. |
| Performance | Yes | Designed for 30W, to work in LTPoE++ standard, if this condition is not met, the overall power budget of the board is affected. |
| Compliance | NA |  |

**Table 17. Impact of Failure – Voltage Accuracy**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| VPORTA\_P | C1811.1 |
| PV18POE | C3M103.1 |
| VSLRPOE\_VOUT | C3M171.1 |
| VPS\_VOUT | C1685.1 |
| VPOUT\_BUCK | C3M96.1 |

**Table 18. Measurement Locations – Voltage Accuracy**

##### **Test Equipment List**

1. LTPoE++ PSE injector - PS-201G++

2. Digital Oscilloscope: MSO9404A

##### **Equipment Settings**

1. LTPoE++ PSE injector - PS-201G++

Supply Voltage: 56V

Current Limit: 1.6A

1. Oscilloscope: MSO9404A

Voltage per division: 5V

Bandwidth: 20MHz

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 56V | Nominal injector input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 19. Test Condition – Voltage Accuracy**

##### **DUT Settings**

1. Isolated input side of Tiva controller by removing the resistor R10054.
2. Isolated input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **Measurement location** | **Range** |
| Input Voltage (V) | C1811.1 | 56V |
| 48V-18V buck converter Output | C3M103.1 | 10.8 - 28V |
| Output voltage of U91 | C1685.1 | Working condition: Should follow the input voltage i.e. 18V |
| Buck-Boost Input voltage(V) | C3M96.1 | Working condition:  Should follow output of U91 i.e. 18V |

**Table 20. Requirements – Voltage Accuracy**

##### **Test Procedure**

1. Remove resistor R10067 and R10054 in order to isolate Intel processor and TIVA respectively.
2. A constant input voltage of 56V is given from PoE injector (PS-201G++) to J1A connector.
3. Measure the output voltage at C3M103.1, C3M171.1, C1685.1 and C3M96.1.

##### **Reference**

Further details can be found in Page 41 and 43 of GBC schematic Ver. Life-2.

#### Test Case: Input Supply Range (Test ID: FP.3.2)

##### **Description**

1. **Purpose**

PoE input supply range must comply with LTPoE++ standard, i.e. it is designed to work in the range of 53.75V to 56V. The purpose of the test case is to validate the range for LTPoE++ voltage range for which GBC will be functional.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | If the voltage range is not between 53.75V to 56V, then the GBC will not be in LTPoE++ standard. |
| Performance | Yes | Designed for 30W, to work in LTPoE++ standard, if this condition is not met, the overall power budget of the board is affected. |
| Compliance | NA |  |

**Table 21. Impact of Failure – Input Supply Range**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| VPORTA\_P | C2005.1 |
| VSLRPOE\_VOUT | C3M171.1 |

**Table 22. Measurement Locations – Input Supply Range**

##### **Test Equipment List**

1. LTPoE++ PSE injector - PS-201G++

2. Digital Oscilloscope: MSO9404A

##### **Equipment Settings**

1. LTPoE++ PSE injector - PS-201G++

Supply Voltage: 53.75 to 56V

Current Limit: 1.6A

1. Oscilloscope: MSO9404A

Voltage per division: 5V

Bandwidth: 20MHz

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 53.75V to 56V | Injector input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 23. Test Condition – Input Supply Range**

##### **DUT Settings**

1. Isolated input side of Tiva controller by removing the resistor R10054.
2. Isolated input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **Measurement location** | **Range** |
| Input Voltage (V) | C2005.1 | 53.75V to 56V |
| Output voltage of U38 | C3M171.1 | Working condition: Should be equal to 18V |

**Table 24. Requirements – Input Supply Range**

##### **Test Procedure**

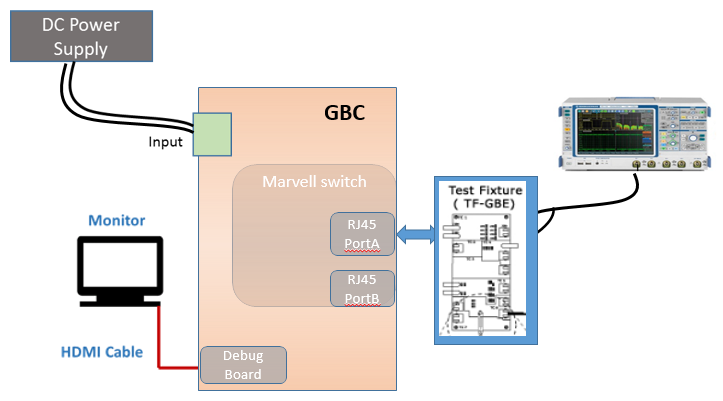
1. Remove resistor R10067 and R10054 in order to isolate Intel processor and TIVA respectively.
2. Vary the input voltage of PoE injector from 53.75V to 56V in steps of 1V. Measure the input voltage at C1811.1.
3. Load GBC up to 30W using an external electronic load.
4. For every change in input voltage, measure the output voltage of 48V to 18V isolated converter (U38) at C3M171.1 and should read 18V.

##### **Reference**

Further details can be found in Page 41 and 43 of GBC schematic Ver. Life-2.

### PoE – Data

#### Test Setup

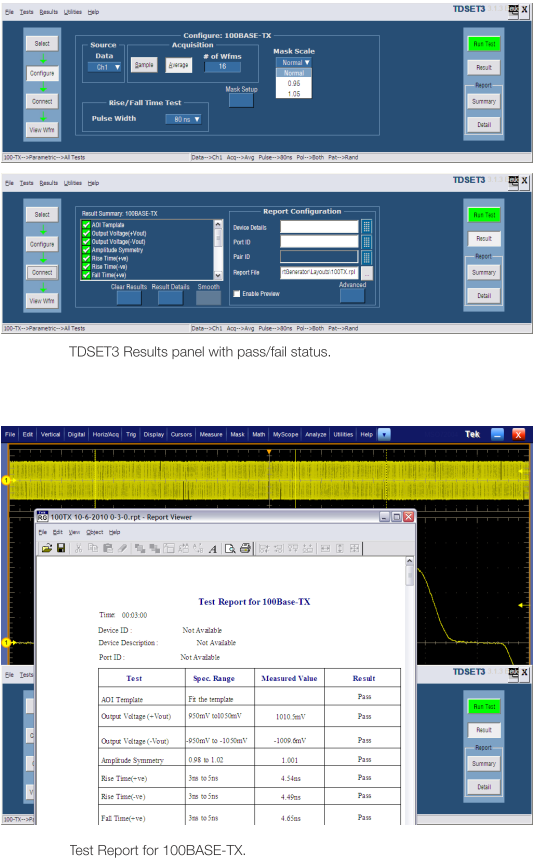


#### Test Case: Ethernet Compliance (Test ID: FP.5.1)

The test procedure and test setup for Ethernet compliance has been performed as per IEEE 802.3 standards and comprises of Template, Differential Output Voltage, Amplitude Symmetry, Rise Time, Fall Time, Rise/Fall Time Symmetry, Waveform Overshoot, Jitter, Duty Cycle Distortion and return loss.

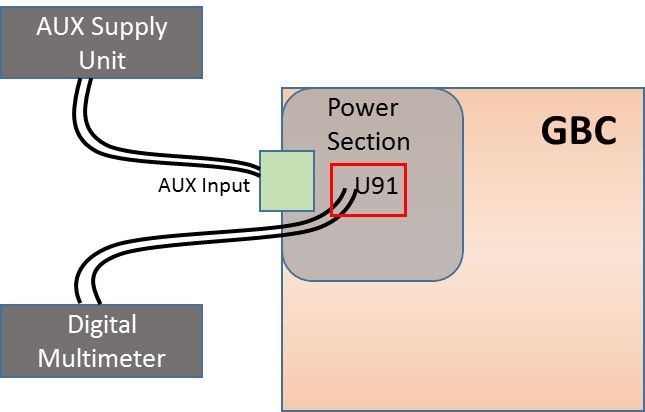
1. Use TC2 of the test fixture for this test. Make the connections as shown in the above diagram
2. Set the DUT to transmit scrambled idles
3. Connect the Ethernet cable to J490 and test port of the DUT
4. Connect the Differential Probe to P9 and configured channel of the oscilloscope
5. Select the test to be performed and click “Run Test” in TDSET3 Ethernet compliance software
6. For return loss measurement, Use TC1 of the test fixture and ensure calibration for “OPEN”, “LOAD” and “SHORT” is performed before executing on actual DUT
7. Connect the Ethernet cable to J200 and test port of the DUT Connect a BNC Cable to (AWG/AFG)+ and Channel 1 of Arbitrary Waveform Generator/Arbitrary Function Generator
8. Connect a BNC Cable to (AWG/AFG)– and Channel 2 of Arbitrary Waveform Generator/Arbitrary Function Generator
9. To test Transmitter, connect the Differential Probes to P1 (J240) and P2 (J230), and configured channels of the oscilloscope
10. To test Receiver, connect the Differential Probe to P3 (J241) and P4 (J231), and configured channels of the oscilloscope.





### Protection

#### Test Setup



**Figure 4. Protection - Test Setup Diagram**

#### Test Case: Voltage limit accuracy (Test ID: FP.6.1)

##### **Description**

1. **Purpose**

LT4256 (U91) is used as the protection IC for under voltage and over current protection. This test is to ensure that GBC will not be functional below the designed threshold voltage.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | If input voltage is less than or more than the designed limit, the powering on of GBC will be affected. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 25. Impact of Failure – Voltage Limit Accuracy**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| VSLRPOE\_VOUT | C3M171.1 |
| VPS\_VOUT | R1056.1 |
| Node voltage at UV pin of U91 | R1053.2 |
| VPOUT\_BUCK | R10071.1 |

**Table 26. Measurement Locations – Voltage Limit Accuracy**

##### **Test Equipment List**

1. AUX Power supply unit: Agilent E3634A

2. Digital Oscilloscope: MSO9404A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 24V

Current Limit: 1.5A

OVP: 26V

OCP: 2A

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50ms

Bandwidth: 20MHz

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 27. Test Condition – Voltage Limit Accuracy**

##### **DUT Settings**

1. Isolated input side of Tiva controller by removing the resistor R10054.
2. Isolated input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **Measurement location** | **Range** |
| Input Voltage (V) | C3M171.1 | 10.5V to 11.5V |
| Node voltage at UV pin of U91 | R1053.2 | Working condition: >3.96 V |
| Output voltage(V) of U91 | R1056.1 | Working condition: Should follow the input voltage |
| Buck-Boost output voltage(V) | R10071.1 | 12V |

**Table 28. Requirements – Voltage Limit Accuracy**

##### **Test Procedure**

1. Remove resistor R10067 and R10054 in order to isolate Intel processor and TIVA respectively.
2. Set the AUX power supply to give a voltage in the range of 10.5V to 11.5V.
3. Varying the AUX supply settings for voltages in steps of 0.2V, measure the input voltage at C3M171.1.
4. Measure nodal voltage at R1053.2. If measured voltage is less than 3.96V, then the IC is in under voltage protection mode. The measured voltage should be greater than 3.96V for normal operation.

##### **Reference**

Further details can be found in Page 48 of GBC schematic Ver. Life-2.

#### Test Case: Solar AUX Present test (Test ID: FP.6.2)

##### **Description**

1. **Purpose**

This test to conclude if Solar or AUX power is being used to power up the GBC board.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | GBC will not be powered up if Solar/Aux is absent and SOLAR\_AUX\_PRSNT\_N is high |
| Performance | Yes | If Solar/Aux voltage source is not detected, the powering of GBC will be affected. |
| Compliance | NA | NA |

**Table 29. Impact of Failure – Solar AUX Present test**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| VSLRPOE\_VOUT | R988.1 |
| VPS\_VOUT | R1056.1 |
| SOLAR\_AUX\_PRSNT\_N | R9957.2 |

**Table 30. Measurement Locations – Solar AUX Present test**

##### **Test Equipment List**

1. AUX Power supply unit: Agilent E3634A

2. Digital Oscilloscope: MSO9404A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 24V

Current Limit: 1.5A

OVP: 26V

OCP: 2A

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50ms

Bandwidth: 20MHz

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 31. Test Condition – Solar AUX Present test**

##### **DUT Settings**

1. Isolated input side of Tiva controller by removing the resistor R10054.
2. Isolated input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **Measurement location** | **Range** |
| Input Voltage (V) | R988.1 | 18V |
| Solar or AUX supply present\_n | R9957.2 | <0.4V (U15 detects a low at voltage < 0.4V) |
| Output voltage(V) of U91 | R1056.1 | Working condition: Should follow the input voltage |

**Table 32. Requirements – Solar AUX Present test**

##### **Test Procedure**

1. Configure the AUX power supply to give 18V as input to the GBC board.
2. Measure the input voltage at R988.1 and ensure that it is 18V.
3. Measure the voltage at R9957.2. If the voltage is < 0.4V then it indicates that the GBC is powered from Solar or AUX supply. If this voltage is 3.3V then it indicates that Solar or AUX supply is absent.

##### **Reference**

Further details can be found in Page 48 and 63 of GBC schematic Ver. Life-2.

#### Test Case: Protection Limit (Test ID: FP.6.3)

##### **Description**

1. **Purpose**

The purpose of this test case is to ensure the voltage protection limits are as per the designed value, i.e. input voltage to U91 (LT4256) is ≥11.5V.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | If the voltage applied is more than or less than the designed value, power section of GBC will be affected. |
| Performance | NA |  |
| Compliance | NA | NA |

**Table 33. Impact of Failure – Protection Limit**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| VSLRPOE\_VOUT | C3M171.1 |
| VPS\_VOUT | R1056.1 |
| 12V\_IN | R10044.2 |
| Nodal Voltage at UV pin of U91 | R1053.2 |

**Table 34. Measurement Locations – Protection Limit**

##### **Test Equipment List**

1. AUX Power supply unit: Agilent E3634A

2. Digital Oscilloscope: MSO9404A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 10.5V to 11.5V

Current Limit: 1.5A

OVP: 20V

OCP: 2A

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50ms

Bandwidth: 20MHz

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 10.5V to 11.5V | Input voltage range |
| Temperature | +25 C | Normal Room temperature |

**Table 35. Test Condition – Protection Limit**

##### **DUT Settings**

1. Isolated input side of Tiva controller by removing the resistor R10054.
2. Isolated input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **Measurement location** | **Range** |
| Input Voltage (V) | C3M171.1 | 10.5V to 11.5V |
| Output of U91 | R1056.1 | Working condition: Should follow the input voltage |
| Output voltage(V) of U88 | R10044.2 | Working condition: Should be equal to 12V |

**Table 36. Requirements – Protection Limit**

##### **Test Procedure**

1. Set the AUX power supply to give a voltage in the range of 10.5V to 11.5V in steps of 0.2V
2. Measure the input voltage at C3M171.1.
3. Measure the voltage at R1056.1 and R10044.2.
4. Input voltage for U91 should be greater than 11.5V for proper operation of GBC. This test fails if input voltage of U91 (VSLRPOE\_VOUT) is less than 11.5V, or if the nodal voltage at R1053 and R1052 junction is greater than 3.96V.

##### **Reference**

Further details can be found in Page 48 and 53 of GBC schematic Ver. Life-2.

# Power Sub-system

## Test Purpose and Description

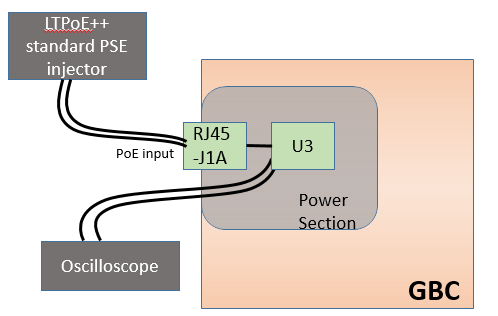
GBC system will have provision for varied power sources to various discrete voltage levels required by devices used in the system. The system also has provision for DC-DC converters for low noise regulated power supply to individual functional blocks and devices

## Power Sub-system constitutes of below components

1. PoE
2. PSE
3. Isolated DC-DC
4. Lead Acid battery
5. Lithium Ion Battery
6. Buck-Boost
7. TIVA power supply
8. 2G module supply
9. FET Switch
10. PMIC
11. System Power sequence

### PoE

#### Test Setup



**Figure 5. PoE- Test Setup Diagram**

#### Test Case: Voltage Accuracy (Test ID: PWR.1.1)

Same as Test Case ID: [FP.3.1](#_Test_Case:_Voltage)

#### Test Case: Ripple Measurement (Test ID: PWR.1.2)

##### **Description**

1. **Purpose**

The purpose of this test case is to check the maximum peak-to-peak ripple voltage of PoE supply.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | If ripple voltage is more than expected, board noise will increase and leading to failure of capacitors. |
| Compliance | NA |  |

**Table 37. Impact of Failure – Ripple Measurement**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| PV18POE | C3M103.1 |

**Table 38. Measurement Locations – Ripple Measurement**

##### **Test Equipment List**

1. LTPoE++ PSE injector - PS-201G++

2. Digital Oscilloscope: MSO9404A

##### **Equipment Settings**

1. LTPoE++ PSE injector - PS-201G++

Supply Voltage: 56V

Current Limit: 1.6A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 56V | Nominal injector input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 39. Test Condition – Ripple Measurement**

##### **DUT Settings**

1. Isolated input side of Tiva controller by removing the resistor R10054.
2. Isolated input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **Measurement location** | **Range** |
| 48V-18V buck converter Output | C3M103.1 | Working condition:  Output voltage should be equal to 18V. Allowable ripple is 900mV (±5% of 18V) |

**Table 40. Requirements – Ripple Measurement**

##### **Test Procedure**

1. Remove resistor R10067 and R10054 in order to isolate Intel processor and TIVA respectively.
2. A constant input voltage of 56V is given from PoE injector (PS-201G++) to J1A connector.
3. An Isolated DC-DC converter in turn converts 56V to 18V. Measure the output voltage at C3M103.1.

##### **Reference**

Further details can be found in Page 43 and 48 of GBC schematic Ver. Life-2.

#### Test Case: Supply Present Check (Test ID: PWR.1.3)

##### **Description**

1. **Purpose**

The purpose of this test case is to check the presence of PoE as an input supply source.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | GBC will not be powered up if PoE supply is absent and PoE\_PRSNT\_N is high (given Solar and Aux input is absent) |
| Performance | Yes | If Solar/Aux voltage source is not detected, the powering of GBC will be affected. (given Solar and Aux input is absent) |
| Compliance | NA | NA |

**Table 41. Impact of Failure – Supply Present Check**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| POE\_PRSNT\_N | R9953.2 |

**Table 42. Measurement Locations – Supply Present Check**

##### **Test Equipment List**

1. LTPoE++ PSE injector - PS-201G++

2. Digital Oscilloscope: MSO9404A

##### **Equipment Settings**

1. LTPoE++ PSE injector - PS-201G++

Supply Voltage: 56V

Current Limit: 1.6A

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50ms

Bandwidth: 20MHz

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 56V | Nominal injector input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 43. Test Condition – Supply Present Check**

##### **DUT Settings**

1. Isolated input side of Tiva controller by removing the resistor R10054.
2. Isolated input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **Measurement location** | **Range** |
| Input Voltage (V) | C1811.1 | 56V |
| PoE supply present\_n | R9953.2 | <1.155V (U15 detects a low under this condition) |
| Input voltage(V) of U77 | C3M103.1 | Working condition: Should be equal to 18V |

**Table 44. Requirements – Supply Present Check**

##### **Test Procedure**

1. Remove resistor R10067 and R10054 in order to isolate Intel processor and TIVA respectively.
2. A constant input voltage of 56V is given from PoE injector (PS-201G++) to J1A connector.
3. An Isolated DC-DC converter in turn converts 56V to 18V.
4. When PoE supply is present, the voltage on R9953.2 Resistor should measure <1.155V. Any voltage less than 1.155V is considered as low signal for Tiva thus indicating the presence of PoE supply.

##### **Reference**

Further details can be found in Page 43 and 63 of GBC schematic Ver. Life-2.

#### Test Case: Data Transfer Validation (Test ID: PWR.1.4)

##### **Description**

1. **Purpose**

This test case indicates the data validation between PoE ports A and B.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | If data validation between ports fails, communication with external PC will be not possible. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 45. Impact of Failure – Data Transfer Validation**

1. **Measurement Locations**

NA

##### **Test Equipment List**

1. LTPoE++ PSE injector - PS-201G++

2. Two CPU systems

##### **Equipment Settings**

1. LTPoE++ PSE injector - PS-201G++

Supply Voltage: 56V

Current Limit: 1.6A

##### **Hardware Requisites**

1. GBC board
2. Two test PCs

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 56V | Nominal injector input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 46. Test Condition – Data Transfer Validation**

##### **DUT Settings**

1. Isolated input side of Tiva controller by removing the resistor R10054.
2. Isolated input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

NA

##### **Test Procedure**

1. Remove resistor R10067 and R10054 in order to isolate Intel processor and TIVA respectively.
2. Connect Data In port of PoE injector to CPU1. Connect Port B of GBC to another machine (CPU2). Ping CPU2 from CPU1 and vice versa.
3. The number of packets transferred from CPU1 to CPU2 and vice versa should have a loss of 0%, then data validation through PoE is successful.

##### **Reference**

Further details can be found in Page 43 of GBC schematic Ver. Life-2.

#### Test Case: Power Delivery (Test ID: PWR.1.5)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the power delivery of PoE.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | The System will not turn on if the required power is not delivered. |
| Compliance | NA |  |

**Table 47. Impact of Failure of PoE Power delivery**

1. **Measurement Locations**

R10044

##### **Test Equipment List**

1. LTPoE++ PSE injector - PS-201G++
2. DC power supply: E3633A

##### **Equipment Settings**

1. LTPoE++ PSE injector - PS-201G++

Supply Voltage: 56V

Current Limit: 1.6A

1. DC power supply: E3633A

Supply Voltage: 56V

Current Limit: 1.5A

OVP: 57V

OCP: 2A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 56V | Nominal injector input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 48. Test Condition – PoE Power delivery**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |
| --- | --- | --- | --- |
| Sl.No. | Parameters | Input Section | Output Section |
| 1 | Probing points | NA | R10044 |
| 2 | Resistor Value (mΩ) | NA | 10 |
| 3 | Voltage (V) | 47.97 | 12 |
| 4 | Expected Power (W) | Output power = Input power | |
| 5 | Expected Efficiency (%) | 60 – 70 (Considering 1A load) | |

**Table 49. Requirements – PoE Power delivery**

##### **Test Procedure**

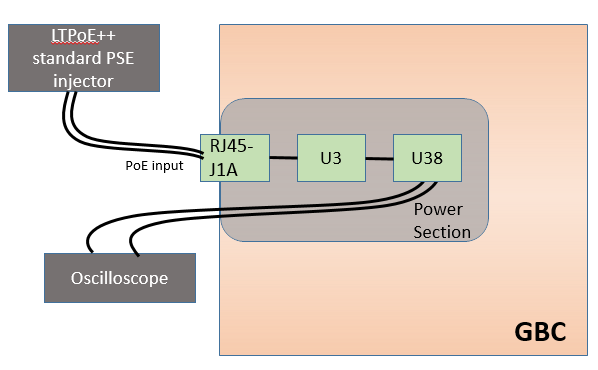
1. Configure DC power supply to give a voltage of 56V.
2. Measure PoE Voltage and Current by connecting input of the PoE injector to DC power supply.
3. Measure the voltage at the output point of injector for input section.
4. Measure the voltage at the sense resistor R10044 for output section.
5. Calculate the current, power and efficiency.
6. The efficiency is calculated as η = 100% \* Pout / Pin.
7. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 43 of GBC schematic Ver. Life-2.

### Isolated DC-DC

#### Test Setup



**Figure 6. Isolated DC-DC - Test Setup Diagram**

#### Test Case: Output Voltage accuracy (Test ID: PWR.3.1)

##### **Description**

1. **Purpose**

The purpose of this test case is to check the voltage accuracy of output voltage rail of DC – DC converter when PoE input voltage is varied.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | If input voltage is less than or more than the designed limit, the power source for GBC will be affected. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 50. Impact of Failure – Output Voltage Accuracy**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| VPORTA\_P | C2005.1 |
| PV18POE | C1807.1 |

**Table 51. Measurement Locations – Output Voltage Accuracy**

##### **Test Equipment List**

1. LTPoE++ PSE injector - PS-201G++

2. Digital Oscilloscope: MSO9404A

##### **Equipment Settings**

1. LTPoE++ PSE injector - PS-201G++

Supply Voltage: 56V

Current Limit: 1.6A

1. Oscilloscope: MSO9404A

Voltage per division: 5V

Bandwidth: 20MHz

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 56V | Nominal injector input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 52. Test Condition – Output Voltage Accuracy**

##### **DUT Settings**

1. Isolated input side of Tiva controller by removing the resistor R10054.
2. Isolated input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **Measurement location** | **Range** |
| Input Voltage (V) | C2005.1 | 56V |
| 48V-18V buck converter Output | C1807.1 | 18V typical |

**Table 53. Requirements – Output Voltage Accuracy**

##### **Test Procedure**

1. Remove resistor R10067 and R10054 in order to isolate Intel processor and TIVA respectively.
2. A constant input voltage of 56V is given from PoE injector (PS-201G++) to J1A connector. Measure the input voltage at C2005.1.
3. Measure the output voltage of DC-DC converter at C1807.1.

##### **Reference**

Further details can be found in Page 47 of GBC schematic Ver. Life-2.

#### Test Case: Solar AUX and PoE OR-ing Circuit (Test ID: PWR.3.2)

##### **Description**

1. **Purpose**

The purpose of this test case is to check the switching between AUX/ Solar supply and PoE supply.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | GBC might be non-operational if switching between AUX/Solar and PoE is not detected properly. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 54. Impact of Failure – Output Voltage Accuracy**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| VSLR\_OVUVOUT | C3M102.1 |
| PV18POE | C1807.1 |
| VSLRPOE\_VOUT | C3M171.1 |

**Table 55. Measurement Locations – Output Voltage Accuracy**

##### **Test Equipment List**

1. LTPoE++ PSE injector - PS-201G++
2. Digital Oscilloscope: MSO9404A
3. AUX Power supply unit: Agilent E3634A

##### **Equipment Settings**

1. LTPoE++ PSE injector - PS-201G++

Supply Voltage: 56V

Current Limit: 1.6A

1. DC power supply: E3633A

Supply Voltage: 15V to 24V

Current Limit: 1.5A

OVP: 26V

OCP: 2A

1. Oscilloscope: MSO9404A

Voltage per division: 5V

Bandwidth: 20MHz

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 56V and 15V to 24V | Nominal injector input voltage and AUX/Solar power supply |
| Temperature | +25 C | Normal Room temperature |

**Table 56. Test Condition – Output Voltage Accuracy**

##### **DUT Settings**

1. Isolated input side of Tiva controller by removing the resistor R10054.
2. Isolated input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **Measurement location** | **Range** |
| AUX / Solar Input Voltage (V) | C3M102.1 | 15V to 24V |
| 48V-18V buck converter Output | C1807.1 | 18V typical |
| Output of OR-ing circuit U77(V) | C3M171.1 | NA |

**Table 57. Requirements – Output Voltage Accuracy**

##### **Test Procedure**

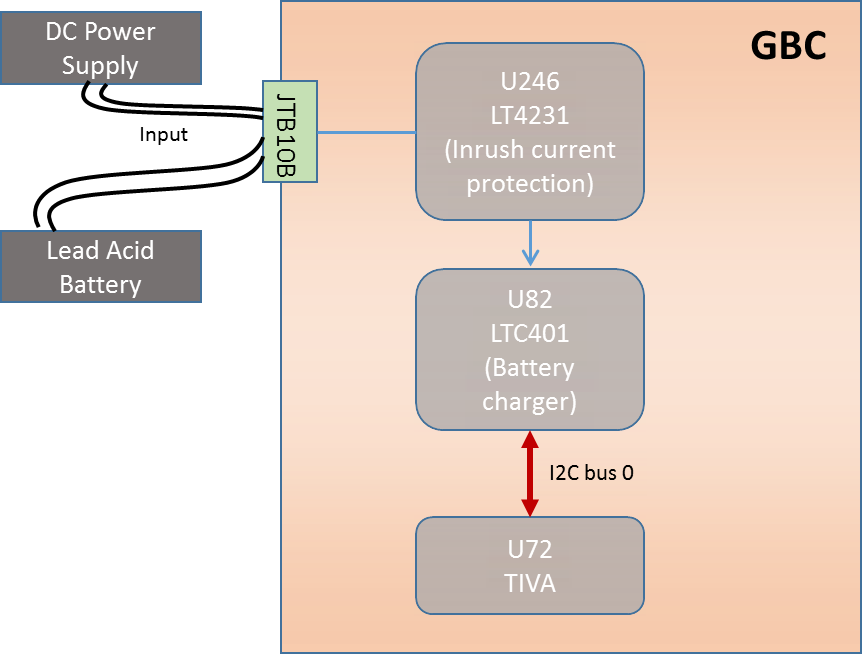
1. Remove resistor R10067 and R10054 in order to isolate Intel processor and TIVA respectively.
2. A constant input voltage of 56V is given from PoE injector (PS-201G++) to J1A connector. Measure the voltage at C1807.1 (18V). Varying AUX / Solar input voltage is also given at JTB10A.1. Measure the input voltage at C3M102.1
3. Output voltage should follow AUX/ Solar supply if AUX supply is greater than 16.3V; else output voltage will follow PoE. Measure the output voltage of DC-DC converter at C3M171.1.

##### **Reference**

Further details can be found in Page 47 and 48 of GBC schematic Ver. Life-2.

### Lead Acid Battery

#### Test Setup



**Figure 7. Lead Acid battery - Test Setup Diagram**

#### Impact of failure of test case on system

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Battery charging and discharging will be affected. |
| Performance | Yes | If GBC is not powered through AUX or PoE, then power supply should be switched to lead acid battery, else device will not be functional. |
| Compliance | NA | NA |

**Table 58. Impact of Failure – Lead Acid battery**

#### Test Case: Output Voltage Accuracy (Test ID: PWR.4.1)

##### **Description**

1. **Purpose**

The purpose of this test case is to check the output voltage accuracy of battery charger U82 (LTC4015).

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement Location** |
| VPS\_VOUT | C1685.1 |
| LACID\_VBAT\_P | JTB10B.3 |
| LT4231\_BAT\_CHRGR\_LACID | C1741.1 |
| VBC\_LACID | C1686.1 |

**Table 59. Measurement Locations – Lead Acid Battery Output Voltage Accuracy**

##### **Test Equipment List**

1. Lead Acid Battery: 65Ah – Amaron Quanta 12AL065

2. Oscilloscope: MSO9404A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 5V

Time scale: 50ms

Bandwidth: 20MHz

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Battery Voltage | 12V | Nominal battery voltage. Varies from 9.5V to 13.8V |
| Temperature | +25 C | Normal Room temperature |

**Table 60. Test Condition – Lead Acid Battery Output Voltage Accuracy**

##### **DUT Settings**

1. Isolate input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **JTB10B.3** | **C1686.1** |
| Battery Voltage(V) | 9.5V to 13.8V | 9.5V to 13.8V |

**Table 61. Requirements - Lead Acid Battery Output Voltage Accuracy**

##### **Test Procedure**

1. Remove resistor R10067 in order to isolate Intel processor.
2. Connect lead acid battery terminals between to JTB10B.3and JTB10B.4
3. Measure the battery voltage at JTB10B.3.
4. The above measured voltage should be equal to the output of the battery charger U82 measured at C1686.1 to ensure proper functionality of GBC module.

##### **Reference**

Further details can be found in Page 49 of GBC schematic Ver. Life-2.

#### Test Case: Charge Current Measurement (Test ID: PWR.4.2)

##### **Description**

1. **Purpose**

Charge current for lead acid battery is designed for 10.6A.

i.e.

Charge current read from register Ibat having sub-address 0x3D, must be equal to the programmed charge current (10.66A).

**Note:** Charge current will decrease when charging voltage increases.

1. **Measurement Locations**

NA

##### **Test Equipment List**

1. Lead Acid Battery: 65Ah – Amaron Quanta 12AL065

2. CCS software

3. AUX Power supply unit: Agilent E3634A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 2.0A

OVP: 20V

OCP: 2.5A

##### **Hardware Requisites**

1. GBC board
2. Debug board

##### **Software Requisites**

1. TIVA RTOS code for lead acid battery configuration

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Battery Voltage | 12V | Nominal battery voltage. Varies from 9.5V to 13.8V |
| Temperature | +25 C | Normal Room temperature |

**Table 62. Test Condition – Lead Acid Battery Charge Current Measurement**

##### **DUT Settings**

1. Isolate input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

Access TIVA (U72) I2C channel 0 through CCS software. Program the charge current for 10.66A by writing to register 0x1A. Read back the charge current from register 0x3D.

Programmed charge current must be equal to read charge current.

**Note:** Charge current will decrease when charging voltage increases.

##### **Test Procedure**

1. Remove resistor R10067 in order to isolate Intel processor.
2. Connect lead acid battery terminals between to JTB10B.3and JTB10B.4
3. Connect a debug board to GBC board in order to access TIVA through CCS.
4. Through I2C channel 0, lead acid battery charger U82 can be accessed. Program the charge current as 10.66A by writing into I*charge \_target* register at address 0x1A.
5. Read register I*bat* having sub-address 0x3D. This value gives the charging current of the lead acid battery.
6. Repeat the same procedure for different values such as 2A, 4A, 6A and 8A as charge current for verification.
7. Measure the charging current by measuring voltage across R9959. Charging current can be calculated by:

##### **Reference**

Further details can be found in Page 49 of GBC schematic Ver. Life-2.

#### Test Case: Load Current Measurement (Test ID: PWR.4.3)

##### **Description**

1. **Purpose**

The purpose of this test case is to measure the current drawn from the battery when system is powered ON by lead acid battery.

1. **Measurement Locations**

Access TIVA (U72) I2C channel 0 through CCS software. Read register 0x3E for load current measurement.

##### **Test Equipment List**

1. Lead Acid Battery: 65Ah – Amaron Quanta 12AL065

2. CCS software

3. AUX Power supply unit: Agilent E3634A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 2.0A

OVP: 20V

OCP: 2.5A

##### **Hardware Requisites**

1. GBC board
2. Debug board

##### **Software Requisites**

1. TIVA RTOS code for lead acid battery configuration

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Battery Voltage | 12V | Nominal battery voltage. Varies from 9.5V to 13.8V |
| Temperature | +25 C | Normal Room temperature |

**Table 63. Test Condition – Lead Acid Battery Load Current Measurement**

##### **DUT Settings**

1. Isolate input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

Access TIVA (U72) I2C channel 0 through CCS software.

##### **Test Procedure**

1. Remove resistor R10067 in order to isolate Intel processor.
2. Connect lead acid battery terminals between to JTB10B.3and JTB10B.4
3. Connect a debug board to GBC board in order to access TIVA through CCS.
4. Through I2C channel 0, lead acid battery charger U82 can be accessed.
5. Read register IIN having sub-address 0x3E. This value gives the load current of GBC board.
6. Load current is given by.

##### **Reference**

Further details can be found in Page 49 of GBC schematic Ver. Life-2.

#### Test Case: LDO Output Voltage (Test ID: PWR.4.4)

##### **Description**

1. **Purpose**

The purpose of this test case is to measure the battery charger (U82) internal INTVCC LDO voltage.

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| INT\_VCC\_LACID | C1767.1 |

**Table 64. Measurement Locations – Lead Acid battery LDO Output Voltage**

##### **Test Equipment List**

1. Lead Acid Battery: 65Ah – Amaron Quanta 12AL065

2. Oscilloscope: MSO9404A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 5V

Time scale: 50ms

Bandwidth: 20MHz

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Battery Voltage | 12V | Nominal battery voltage. Varies from 9.5V to 13.8V |
| Temperature | +25 C | Normal Room temperature |

**Table 65. Test Condition – Lead Acid battery LDO Output Voltage**

##### **DUT Settings**

1. Isolate input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |
| --- | --- |
| **Measurement Parameter** | **C1767.1** |
| INTVcc (internal LDO voltage) | 5V |

**Table 66. Requirements – – Lead Acid battery LDO Output Voltage**

##### **Test Procedure**

1. Remove resistor R10067 in order to isolate Intel processor.
2. Connect lead acid battery terminals between to JTB10B.3 and JTB10B.4
3. Measure the battery charger U82 internal LDO output voltage at C1767.1
4. The above measured voltage should be equal to 5V to ensure proper functionality of GBC module.

##### **Reference**

Further details can be found in Page 49 of GBC schematic Ver. Life-2.

#### Test Case: Temperature Measurement (Test ID: PWR.4.5)

##### **Description**

1. **Purpose**

The purpose of this test case is to measure the temperature of battery charger IC U82 when it’s fully operational.

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| Temperature | Internal temperature of U82 |

**Table 67. Measurement Locations – Lead acid battery charger temperature measurement**

##### **Test Equipment List**

1. Lead Acid Battery: 65Ah – Amaron Quanta 12AL065
2. CCS software

##### **Equipment Settings**

NA

##### **Hardware Requisites**

1. GBC board
2. Debug board

##### **Software Requisites**

1. TIVA RTOS code for lead acid battery configuration

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Battery Voltage | 12V | Nominal battery voltage. Varies from 9.5V to 13.8V |
| Temperature | +25 C | Normal Room temperature |

**Table 68. Test Condition – Lead acid battery charger temperature measurement**

##### **DUT Settings**

1. Isolate input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |
| --- | --- |
| **Measurement Parameter** | **U82** |
| Temperature | Within -40o C to +125o C |

**Table 69. Requirements – Lead acid battery charger temperature**

##### **Test Procedure**

1. Remove resistor R10067 in order to isolate Intel processor.
2. Connect lead acid battery terminals between to JTB10B.3and JTB10B.4
3. Connect lead acid battery. Connect a debug board to GBC board in order to access TIVA through CCS. Through I2C channel 0 lead acid battery charger, U82 can be accessed. Read register DIE\_TEMPERATURE having sub-address 0x3F.

##### **Reference**

Further details can be found in Page 49 of GBC schematic Ver. Life-2.

#### Test Case: Charge Control (Test ID: PWR.4.6)

##### **Description**

1. **Purpose**

This test case indicates the programmed charge current for lead acid battery.

1. **Measurement Locations**

NA

##### **Test Equipment List**

1. Lead Acid Battery: 65Ah – Amaron Quanta 12AL065

2. CCS software

3. AUX Power supply unit: Agilent E3634A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 12.0A

OVP: 20V

OCP: 15A

##### **Hardware Requisites**

1. GBC board
2. Debug board

##### **Software Requisites**

1. TIVA RTOS code for lead acid battery configuration

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Battery Voltage | 12V | Nominal battery voltage. Varies from 9.5V to 13.8V |
| Temperature | +25 C | Normal Room temperature |

**Table 70. Test Condition – Lead acid battery charger Charge Control measurement**

##### **DUT Settings**

1. Isolate input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |
| --- | --- |
| **Measurement Parameter** | **U82** |
| ICHARGE\_TARGET | Register 0x1A |

**Table 71. Requirements – Lead acid battery charger Charge Control measurement**

##### **Test Procedure**

1. Remove resistor R10067 in order to isolate Intel processor.
2. Connect lead acid battery terminals between to JTB10B.3and JTB10B.4
3. Connect lead acid battery. Connect a debug board to GBC board in order to access TIVA through CCS. Through I2C channel 0, lead acid battery charger U82 can be accessed.
4. Write the desired charge current to register 0x1A, ICHARGE\_TARGET. Read the register 0x3D to measure the charge current.

##### **Reference**

Further details can be found in Page 49 of GBC schematic Ver. Life-2.

#### Test Case: Lead Acid and Li-ion battery OR-ing circuit (Test ID: PWR.4.7)

##### **Description**

1. **Purpose**

The purpose of this test case is to ensure that power supply will be switched between external battery (Lead acid battery) and internal battery (Lithium - ion battery) at the designed voltage.

Detects Lead acid battery if battery voltage is greater than 11.5V.

Detects Lithium Ion battery if battery voltage is greater than 11.2V.

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| VBC\_LACID | C3M97.1 |
| VBC\_LION | C3M98.1 |

**Table 72. Measurement Locations – Battery OR-ing Circuit**

##### **Test Equipment List**

1. Lead Acid Battery: 65Ah – Amaron Quanta 12AL065
2. Lithium Ion Battery: 3000mAH - LP103090TB

3. Oscilloscope: MSO9404A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 5V

Time scale: 50ms

Bandwidth: 20MHz

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Battery Voltage | 12V | Nominal battery voltage. To be greater than 11.5V |
| Temperature | +25 C | Normal Room temperature |

**Table 73. Test Condition – Battery OR-ing Circuit**

##### **DUT Settings**

1. Isolate input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **C3M97.1** | **C3M98.1** |
| VBC\_LACID | >11.5V | NA |
| VBC\_LION | NA | <11.2V |

**Table 74. Requirements – Battery OR-ing Circuit**

##### **Test Procedure**

1. Remove resistor R10067 in order to isolate Intel processor.
2. Connect lead acid battery terminals between to JTB10B.3and JTB10B.4
3. Measure the battery voltage at JTB10B.3.
4. If lead acid battery voltage is greater than 10.35V then measured voltage at C3M96.1 should be equal to lead acid battery voltage indicating that lead acid battery is present as the power source for GBC.

##### **Reference**

Further details can be found in Page 46 and 52 of GBC schematic Ver. Life-2.

#### Test Case: Power Delivery (Test ID: PWR.4.8)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the power delivery of Lead Acid battery.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | The System will not turn on if the required power is not delivered. |
| Compliance | NA |  |

**Table 75. Impact of Failure of Lead acid battery charger - Power delivery**

1. **Measurement Locations**

R9959, R10044

##### **Test Equipment List**

1. DC power supply: Agilent E3634A
2. Lead Acid Battery: 65Ah – Amaron Quanta 12AL065

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 12.0A

OVP: 20V

OCP: 15A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Battery Voltage | 12V | Nominal battery voltage. Varies from 9.5V to 13.8V |
| Temperature | +25 C | Normal Room temperature |

**Table 76. Test Condition – Lead acid battery charger - Power delivery**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |
| --- | --- | --- | --- |
| Sl. No. | Parameters | Input Section | Output Section |
| 1 | Probing points | R9959 | R10044 |
| 2 | Resistor Value (mΩ) | 5 | 10 |
| 3 | Voltage (V) | 11.89 | 12 |
| 6 | Expected Power (W) | Output power = Input power | |
| 7 | Expected Efficiency (%) | 60 – 70 (Considering 1A load) | |

**Table 77. Requirements – Lead acid battery charger - Power delivery**

##### **Test Procedure**

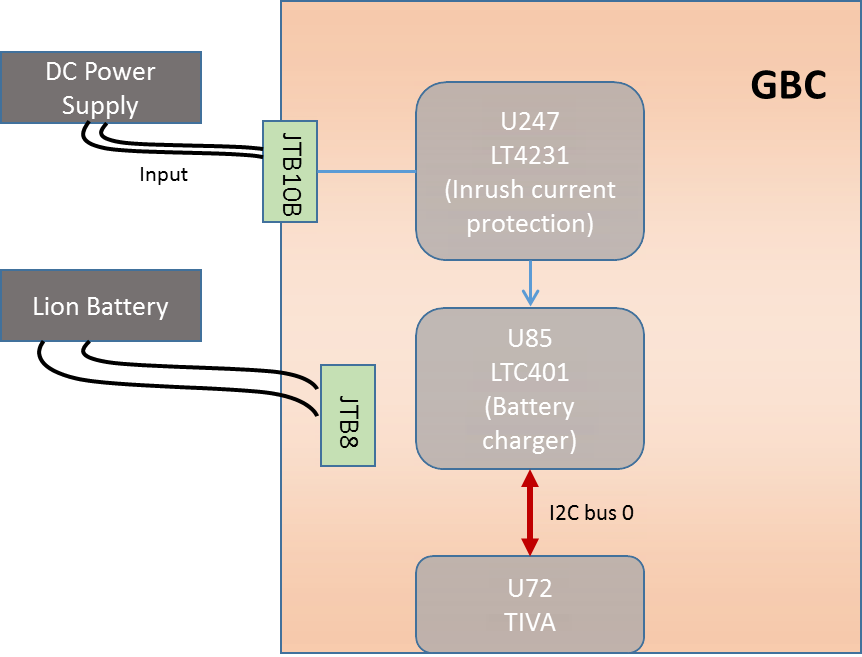
1. Connect lead acid battery terminals between JTB10B.3 and JTB10B.4 of GBC board.
2. Configure DC power supply to give a voltage of 18V.
3. Measure the voltage at the sense resistors R9959 (for input section) and R10044 (output section)
4. Calculate the current, power and efficiency.
5. The efficiency is calculated as η = 100% \* Pout / Pin.
6. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 49 of GBC schematic Ver. Life-2.

### Lithium Ion Battery

#### Test Setup



**Figure 8. Lithium Ion battery - Test Setup Diagram**

#### Impact of failure of test case on system

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Battery charging and discharging will be affected. |
| Performance | Yes | If GBC is not powered through AUX or PoE, then power supply should be switched to lithium ion battery, else device will not be functional. |
| Compliance | NA | NA |

**Table 78. Failure Impact – Lithium Ion Battery Output Voltage Accuracy**

#### Test Case: Output Voltage Accuracy (Test ID: PWR.5.1)

##### **Description**

1. **Purpose**

Lithium ion battery is designed to work from voltage greater than 11.2V when AUX or solar input supply is absent. The purpose of this test case is to ensure the output voltage accuracy is within the desired level.

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| LT4231\_LION\_P | JTB8.1 |
| VBC\_LION | C1717.1 |

**Table 79. Measurement Locations – Lithium Ion Battery Output Voltage Accuracy**

##### **Test Equipment List**

1. Lithium Ion Battery: 3000mAH - LP103090TB

2. Oscilloscope: MSO9404A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 5V

Time scale: 50ms

Bandwidth: 20MHz

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Battery Voltage | 11.2V | Nominal battery voltage. Varies from 9V to 12.6V |
| Temperature | +25 C | Normal Room temperature |

**Table 80. Test Condition – Lithium Ion Battery Output Voltage Accuracy**

##### **DUT Settings**

1. Isolate input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |  |  |
| --- | --- | --- | --- |
| **Measurement Parameter** | **JTB8.1** | **C1715.1** | **C1718.1** |
| Battery Voltage(V) | 9V to 12.6V | 9V to 12.6V | 18V |

**Table 81. Requirements – Lithium Ion Battery Output Voltage Accuracy**

##### **Test Procedure**

1. Remove resistor R10067 in order to isolate Intel processor.
2. Connect lithium ion battery terminals between to JTB8.1 and JTB8.2
3. Measure the battery voltage at JTB8.1
4. The above measured voltage should be equal to the output of the battery charger U85 measured at C1715.1 and C1718.1 to ensure proper functionality of GBC module.

##### **Reference**

Further details can be found in Page 50 of GBC schematic Ver. Life-2.

#### Test Case: Charge Current Measurement (Test ID: PWR.5.2)

##### **Description**

1. **Purpose**

Charge current for lithium ion battery is designed for 1.45A.

i.e.

Charge current read from register I*bat* having sub-address 0x3D, must be equal to the programmed charge current (1.45A).

**Note:** Charge current will decrease when charging voltage increases.

1. **Measurement Locations**

Access TIVA (U72) I2C channel 0 through CCS software. Read back the charge current from register 0x3D. Measure the current across R10039.

##### **Test Equipment List**

1. Lithium Ion Battery: 3000mAH - LP103090TB

2. CCS software

3. AUX Power supply unit: Agilent E3634A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 2.0A

OVP: 20V

OCP: 2.5A

##### **Hardware Requisites**

1. GBC board
2. Debug board

##### **Software Requisites**

1. TIVA RTOS code for lead acid battery configuration

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Battery Voltage | 11.2V | Nominal battery voltage. Varies from 9V to 12.6V |
| Temperature | +25 C | Normal Room temperature |

**Table 82. Test Condition – Lithium Ion Battery Output Voltage Accuracy**

##### **DUT Settings**

1. Isolate input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

Access TIVA (U72) I2C channel 0 through CCS software. Program the charge current for 1.45A by writing to register 0x1A. Read back the charge current from register 0x3D.

Programmed charge current must be equal to read charge current.

**Note:** Charge current will decrease when charging voltage increases.

##### **Test Procedure**

1. Remove resistor R10067 in order to isolate Intel processor.
2. Connect lithium ion battery terminals between to JTB8.1 and JTB8.2
3. Connect a debug board to GBC board in order to access TIVA through CCS.
4. Through I2C channel 0, lithium ion battery charger U85 can be accessed.
5. Read register Ibat having sub-address 0x3D. This value gives the charging current of the lithium ion battery. Read value must be equal to the measured current across R10039.

##### **Reference**

Further details can be found in Page 50 of GBC schematic Ver. Life-2.

#### Test Case: Load Current Measurement (Test ID: PWR.5.3)

##### **Description**

1. **Purpose**

Load current measurement is done by reading register *IIN* having sub-address 0x3E. Load current measured must be greater than charge current measured.

1. **Measurement Locations**

Access TIVA (U72) I2C channel 0 through CCS software. Read register 0x3E for load current measurement.

##### **Test Equipment List**

1. Lithium Ion Battery: 3000mAH - LP103090TB

2. CCS software

3. AUX Power supply unit: Agilent E3634A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 2.0A

OVP: 20V

OCP: 2.5A

##### **Hardware Requisites**

1. GBC board
2. Debug board

##### **Software Requisites**

1. TIVA RTOS code for lead acid battery configuration

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Battery Voltage | 11.2V | Nominal battery voltage. Varies from 9V to 12.6V |
| Temperature | +25 C | Normal Room temperature |

**Table 83. Test Condition – Lithium Ion Battery Load Current Measurement**

##### **DUT Settings**

1. Isolate input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

Access TIVA (U72) I2C channel 0 through CCS software.

##### **Test Procedure**

1. Remove resistor R10067 in order to isolate Intel processor.
2. Connect lithium ion battery terminals between to JTB8.1 and JTB8.2
3. Connect a debug board to GBC board in order to access TIVA through CCS.
4. Through I2C channel 0, Lithium Ion battery charger U85 can be accessed.
5. Read register IIN having sub-address 0x3E. This value gives the load current of GBC board.
6. Measure the current across R9961.

##### **Reference**

Further details can be found in Page 50 of GBC schematic Ver. Life-2.

#### Test Case: LDO Output Voltage (Test ID: PWR.5.4)

##### **Description**

1. **Purpose**

The purpose of this test case is to ensure the internal LDO output voltage of Lithium Ion battery charger U85 must be equal to 5V.

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| INT\_VCC\_LION | C1765.1 |

**Table 84. Measurement Locations – Lithium Ion Charger LDO Output Voltage**

##### **Test Equipment List**

1. Lithium Ion Battery: 3000mAH - LP103090TB

2. Oscilloscope: MSO9404A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 5V

Time scale: 50ms

Bandwidth: 20MHz

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

1. TIVA RTOS code for lead acid battery configuration

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Battery Voltage | 11.2V | Nominal battery voltage. Varies from 9V to 12.6V |
| Temperature | +25 C | Normal Room temperature |

**Table 85. Test Condition – Lithium Ion Charger LDO Output Voltage**

##### **DUT Settings**

1. Isolate input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |
| --- | --- |
| **Measurement Parameter** | **C1765.1** |
| INTVcc (internal LDO voltage) | 5V |

**Table 86. Requirements – Lithium Ion Charger LDO Output Voltage**

##### **Test Procedure**

1. Remove resistor R10067 in order to isolate Intel processor.
2. Connect lithium ion battery terminals between to JTB8.1 and JTB8.2
3. Measure the battery charger U85 internal LDO output voltage at C1765.1
4. The above measured voltage should be equal to 5V to ensure proper functionality of GBC module.

##### **Reference**

Further details can be found in Page 50 of GBC schematic Ver. Life-2.

#### Test Case: Temperature Measurement (Test ID: PWR.5.5)

##### **Description**

1. **Purpose**

The purpose of this test case is to measure the temperature of battery charger IC U85 when it’s fully operational.

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| Temperature | Of U85 |

**Table 87. Measurement Locations – Lithium Ion battery charger temperature measurement**

##### **Test Equipment List**

1. Lithium Ion Battery: 3000mAH - LP103090TB
2. CCS software

##### **Equipment Settings**

NA

##### **Hardware Requisites**

1. GBC board
2. Debug board

##### **Software Requisites**

1. TIVA RTOS code for lead acid battery configuration

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Battery Voltage | 12V | Nominal battery voltage. Varies from 9.5V to 12.6V |
| Temperature | +25 C | Normal Room temperature |

**Table 88. Test Condition – Lead acid battery charger temperature measurement**

##### **DUT Settings**

1. Isolate input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |
| --- | --- |
| **Measurement Parameter** | **U82** |
| Temperature | Within -40o C to +125o C |

**Table 89. Requirements – Lead acid battery charger temperature measurement Test**

##### **Procedure**

1. Remove resistor R10067 in order to isolate Intel processor.
2. Connect lithium ion battery terminals between to JTB8.1 and JTB8.2
3. Connect a debug board to GBC board in order to access TIVA through CCS. Through I2C channel 0, lithium ion battery charger U85 can be accessed.
4. Read register DIE\_TEMPERATURE having sub-address 0x3F.

##### **Reference**

Further details can be found in Page 50 of GBC schematic Ver. Life-2.

#### Test Case: Charge Control (JEITA) (Test ID: PWR.5.6)

##### **Description**

1. **Purpose**

This test case indicates the current at which the lithium ion battery should be charged at a given temperature.

1. **Measurement Locations**

NA

##### **Test Equipment List**

1. Lithium Ion Battery: 3000mAH - LP103090TB
2. CCS software
3. AUX Power supply unit: Agilent E3634A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 3.0A

OVP: 20V

OCP: 4A

##### **Hardware Requisites**

1. GBC board
2. Debug board

##### **Software Requisites**

1. TIVA RTOS code for lithium ion battery configuration

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Battery Voltage | 12V | Nominal battery voltage. Varies from 9.5V to 13.8V |
| Temperature | +25 C | Normal Room temperature |

**Table 90. Test Condition – Lithium Ion battery charger temperature measurement**

##### **DUT Settings**

1. Isolate input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |
| --- | --- |
| **Measurement Parameter** | **U82** |
| IBAT | Register 0x3D |

**Table 91. Requirements – Lithium Ion battery charger temperature measurement**

##### **Test Procedure**

1. Remove resistor R10067 in order to isolate Intel processor.
2. Connect lithium ion battery terminals between to JTB8.1 and JTB8.2
3. Connect a debug board to GBC board in order to access TIVA through CCS. Through I2C channel 0, Lithium Ion battery charger U85 can be accessed.
4. Write to registers from JEITA\_T1 (sub- address 0x1F) to JEITA\_T6 (sub- address 0x24) with temperature range from 0◦C to 60◦C.
5. Read register DIE\_TEMP (sub-address 0x3F) to know the temperature. The battery should charge with a current corresponding to the measured temperature.
6. Measure the charging current by measuring voltage across R10039. Charging current can be calculated by: . Also read the register IBAT (sub-address 0x3D).

##### **Reference**

Further details can be found in Page 49 of GBC schematic Ver. Life-2.

#### Test Case: Lead Acid and Li-ion battery OR-ing circuit (Test ID: PWR.5.7)

##### **Description**

1. **Purpose**

The purpose of this test case is to ensure that power supply will be switched between external battery (Lead acid battery) and internal battery (Lithium - ion battery) at the designed voltage. Detects Lead acid battery if battery voltage is greater than10.35V. Detects Lithium Ion battery if battery voltage is greater than 11.2V.

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| VBC\_LACID | C3M97.1 |
| VBC\_LION | C3M98.1 |
| VPOUT\_BUCK | C3M96.1 |

**Table 92. Measurement Locations – Battery OR-ing Circuit**

##### **Test Equipment List**

1. Lead Acid Battery: 65Ah – Amaron Quanta 12AL065
2. Lithium Ion Battery: 3000mAH - LP103090TB
3. Oscilloscope: MSO9404A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 5V

Time scale: 50ms

Bandwidth: 20MHz

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Battery Voltage | 11.2V | Nominal battery voltage. To be greater than 11.2V and lead acid battery voltage < 11.5V |
| Temperature | +25 C | Normal Room temperature |

**Table 93. Test Condition – Battery OR-ing Circuit**

##### **DUT Settings**

1. Isolate input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Measurement Parameter** | **R1274.2** | **R1275.1** | **C3M97.1** | **C3M98.1** |
| VBC\_LACID | NA | NA | <10.35V | NA |
| VBC\_LION | NA | NA | NA | >11.2V |

**Table 94. Requirements – Battery OR-ing Circuit**

##### **Test Procedure**

1. Remove resistor R10067 in order to isolate Intel processor.
2. Connect lithium ion battery terminals between to JTB8.1and JTB8.2
3. Measure the battery voltage at JTB8.1.
4. If lithium ion battery voltage is greater than 11.2V and lead acid battery voltage is less than 10.35V, then measured voltage at VPS\_VOUT at C3M96. Indicating that lithium ion battery is present as the power source for GBC.

##### **Reference**

Further details can be found in Page 46 and 52 of GBC schematic Ver. Life-2.

#### Test Case: Charge Time (Test ID: PWR.5.8)

##### **Description**

1. **Purpose**

Charge time can be programmed by writing into register *MAX\_CHARGE\_TIME* at address 0x1E.

1. **Measurement Locations**

Access TIVA (U72) I2C channel 0 through CCS software. Read *MAX\_CHARGE\_TIMER* register 0x30 to obtain maximum charge time.

##### **Test Equipment List**

1. Lithium Ion Battery: 3000mAH - LP103090TB

2. CCS software

3. AUX Power supply unit: Agilent E3634A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 2.0A

OVP: 20V

OCP: 2.5A

##### **Hardware Requisites**

1. GBC board
2. Debug board

##### **Software Requisites**

1. TIVA RTOS code for lead acid battery configuration

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Battery Voltage | 11.2V | Nominal battery voltage. Varies from 9V to 12.6V |
| Temperature | +25 C | Normal Room temperature |

**Table 95. Test Condition – Lithium Ion Battery Charge Time Measurement**

##### **DUT Settings**

1. Isolate input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

Access TIVA (U72) I2C channel 0 through CCS software.

##### **Test Procedure**

1. Remove resistor R10067 in order to isolate Intel processor.
2. Connect lithium ion battery terminals between to JTB8.1and JTB8.2
3. Connect a debug board to GBC board in order to access TIVA through CCS.
4. Through I2C channel 0, lithium ion battery charger U85 can be accessed.
5. Read register MAX\_CHARGE\_TIME having sub-address 0x30. This register outputs the value of total time (in seconds) the lithium ion battery is in charging state.

##### **Reference**

Further details can be found in Page 50 of GBC schematic Ver. Life-2

#### Test Case: Power Delivery (Test ID: PWR.5.9)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the power delivery of Lithium Ion Battery.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | The System will not turn on if the required power is not delivered |
| Compliance | NA |  |

**Table 96. Impact of Failure of Lithium Ion Battery charger - Power delivery**

1. **Measurement Locations**

R10039, R10044

##### **Test Equipment List**

1. DC power supply: Agilent E3634A
2. Lead Acid Battery: 65Ah – Amaron Quanta 12AL065

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 12.0A

OVP: 20V

OCP: 15A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Battery Voltage | 11.2V | Nominal battery voltage. Varies from 9V to 12.6V |
| Temperature | +25 C | Normal Room temperature |

**Table 97. Test Condition – Lithium Ion Battery charger - Power delivery**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |
| --- | --- | --- | --- |
| Sl.No. | Parameters | Input Section | Output Section |
| 1 | Probing points | R10039 | R10044 |
| 2 | Resistor Value (mΩ) | 22 | 10 |
| 3 | Voltage (V) | 12.48 | 12 |
| 6 | Expected Power (W) | Output power = Input power | |
| 7 | Expected Efficiency (%) | 60 – 70 (Considering 1A load) | |

**Table 98. Requirements – Lithium Ion Battery charger - Power delivery**

##### **Test Procedure**

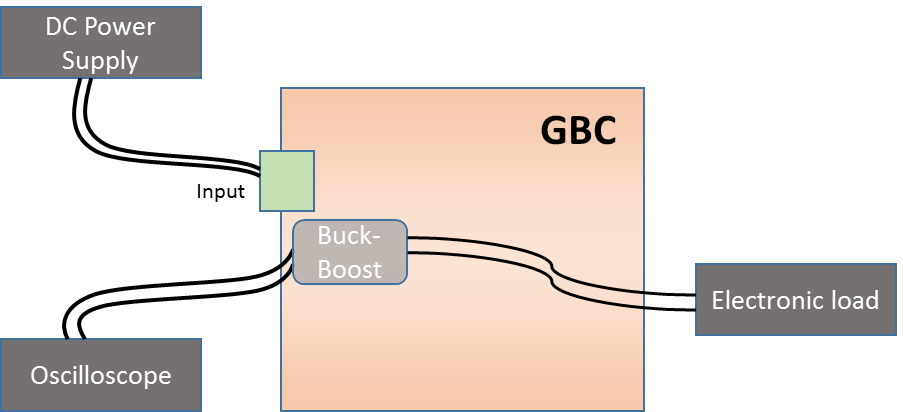
1. Connect lithium ion battery terminals between JTB8.1 and JTB8.2 of GBC board.
2. Configure DC power supply to give a voltage of 18V.
3. Measure the voltage at the sense resistors R10039 (for input section) and R10044 (output section)
4. Calculating the current and power and efficiency.
5. The efficiency is calculated as **η = 100% \* *Pout* / *Pin***.
6. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 50 of GBC schematic Ver. Life-2.

### Buck-Boost

#### Test Setup



**Figure 9. Buck-Boost - Test Setup Diagram**

#### Test Case: line regulation (Test ID: PWR.6.1)

##### **Description**

1. **Purpose**The purpose of this test case is to check the ability of the Buck-Boost converter to maintain its specified output voltage over changes in the input line voltage.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | If the output voltage is not as expected with the varying input voltage, then the end devices will not power up or will get damage. |
| Compliance | NA |  |

**Table 99. Impact of Failure of line regulation**

1. **Measurement Locations**
2. R10044.2

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A
3. Electronic load

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage scale: 5V

1. DC power supply: E3633A

Supply Voltage: +9V DC to 22V DC

Current Limit: 2A

OVP: 23V

OCP: 2.1A

1. Electronic load

Current Limit: 0.5A - 1.5A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | +9V DC to 22V DC | Varied input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 100. Test Condition for line regulation**

##### **DUT Settings**

1. Remove R10071 resistor to isolate input side of buck boost (U88).
2. Remove R10054 and R10067 resistors to isolate output side of buck boost from TIVA and Intel.

##### **Requirements**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Voltage Rail** | **Measuring Point** | **Input Voltage(V)** | **Load current(A)** | **Expected Output Voltage(V)** | **Accuracy/Pass criteria** |
| 12V\_IN | R10044.2 | 9 - 22 | 0.5 – 1.5 | 12 | ±2% |

**Table 101. Requirements for line regulation**

##### **Test Procedure**

1. This test is conducted by configuring power supply to give a voltage in the range of 9V to 22V.
2. Connect load at R10044.2 (output of buck- boost).
3. Vary the input voltage.
4. Vary load current from 0.5 to 1.5 in steps of 0.5.
5. Measure output voltage at R10044.2 and make sure the measured voltage should be within the tolerance limit (±2%) as mentioned in the above requirement table.

##### **Reference**

Further details can be found in Page 53, 55 and 28 of GBC schematic Ver. Life-2.

#### Test Case: Load regulation (Test ID: PWR.6.2)

##### **Description**

1. **Purpose**The purpose of this test case is to check the capability of Buck-Boost converter to maintain a constant output voltage over changes in the load.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | If the output voltage is not as expected with the varying output load, then the end devices will get damage. |
| Compliance | NA |  |

**Table 102. Impact of Failure of load regulation**

1. **Measurement Locations**

R10044.2

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A
3. Electronic load

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage scale: 5V

1. DC power supply: E3633A

Supply Voltage: 18V DC

Current Limit: 2A

OVP: 19V

OCP: 2.1A

1. Electronic load

Current Limit: 0.5A - 1.5A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | +18V DC | Nominal voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 103. Test Condition for load regulation**

##### **DUT Settings**

1. Remove R10071 resistor to isolate input side of buck boost (U88).
2. Remove R10054 and R10067 resistors to isolate output side of buck boost from TIVA and Intel.

##### **Requirements**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Voltage Rail** | **Measuring Point** | **Input Voltage(V)** | **Load current(A)** | **Expected Output Voltage(V)** | **Accuracy/Pass criteria** |
| 12V\_IN | R10044.2 | 18 | 0.5 – 1.5 | 12 | ±2% |

**Table 104. Requirements for load regulation**

##### **Test Procedure**

1. This test is conducted by configuring power supply to give a voltage of 18V.
2. Connect load at R10044.2 (output of buck- boost).
3. Vary load current from 0.5 to 1.5 in steps of 0.5.
4. Measure output voltage at R10044.2 and make sure the measured voltage should be within the tolerance limit (±2%) as mentioned in the above requirement table.

##### **Reference**

Further details can be found in Page 53, 55 and 28 of GBC schematic Ver. Life-2.

#### Test Case: Ripple measurement (Test ID: PWR.6.3)

##### **Description**

1. **Purpose**The purpose of this test case is to check the maximum peak-to-peak ripple voltage of Buck-Boost converter output under different load conditions and input voltage.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | If ripple voltage is more than expected, board noise will increase and leading to failure of capacitors. |
| Compliance | NA |  |

**Table 105. Impact of Failure of Ripple measurement**

1. **Measurement Locations**

C1990

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A
3. Electronic load

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage scale: 100mV

1. DC power supply: E3633A

Supply Voltage: +9V DC to 22V DC

Current Limit: 2A

OVP: 23V

OCP: 2.1A

1. Electronic load

Current Limit: 0.5A - 1.5A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | +9V DC to 22V DC | Varied input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 106. Test Condition for ripple measurement**

##### **DUT Settings**

1. Remove R10071 resistor to isolate input side of buck boost (U88).
2. Remove R10054 and R10067 resistors to isolate output side of buck boost from TIVA and Intel.

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Voltage Rail** | **Measuring Point** | **Input Voltage(V)** | **Load current(A)** | **Maximum Ripple Voltage** |
| 12V\_IN | C1990 | 9V – 22V | 0.5 – 1.5 | ±5%\*input voltage |

**Table 107. Requirements for ripple measurement**

##### **Test Procedure**

1. This test is conducted by configuring power supply to give a voltage in the range of 9V to 22V.
2. Connect load at R10044.2 (output of buck- boost).
3. Vary the input voltage.
4. Vary load current from 0.5 to 1.5 in steps of 0.5.
5. Measure ripple voltage at C1990 and make sure the measured ripple voltage should be less than ±5% of input voltage as mentioned in the above requirement table.

##### **Reference**

Further details can be found in Page 53, 55 and 28 of GBC schematic Ver. Life-2.

#### Test Case: Load current measurement (Test ID: PWR.6.4)

##### **Description**

1. **Purpose**The purpose of this test case is to measure the current drawn by Buck-Boost Converter when it is fully operational.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | NA |  |
| Compliance | NA |  |

**Table 108. Impact of Failure of load current measurement**

1. **Measurement Locations**
2. R10044

##### **Test Equipment List**

1. DC power supply: E3633A
2. Digital multimeter: 34401A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V DC

Current Limit: 1.5A

OVP: 19V

OCP: 1.6A

1. Digital multimeter: 34401A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | +18V DC | Nominal voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 109. Test Condition for load current measurement**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Voltage Rail** | **Measuring Point** | **Input Voltage(V)** | **Expected Load current(A)** | |
| **Min** | **Max** |
| 12V\_IN | R10044 | 18 | 0.4 | 0.8 |

**Table 110. Requirements for load current measurement**

**NOTE: As per the design spec maximum GBC standalone load current is 0.8A.**

##### **Test Procedure**

1. This test is conducted by configuring power supply to give a voltage of 18V.
2. Measure voltage across sense resistor R10044 (0.01ohm).
3. Using measured voltage derive current drawn by the system.
4. Make sure the derived current should match the system load current as mentioned in the above requirement table.

##### **Reference**

Further details can be found in Page 53 of GBC schematic Ver. Life-2.

#### Test Case: Temperature measurement (Test ID: PWR.6.5)

##### **Description**

1. **Purpose**The purpose of this test case is to measure the operating junction temperature of Buck Boost converter when it is fully operational under ambient temperature.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case will result in damage of IC (U88). |
| Performance | NA |  |
| Compliance | NA |  |

**Table 111. Impact of Failure of Temperature****measurement**

1. **Measurement Locations**
2. U88

##### **Test Equipment List**

1. DC power supply: E3633A
2. Fluke 59 Mini IR Thermometer

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V DC

Current Limit: 1.5A

OVP: 19V

OCP: 1.6A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | +18V DC | Nominal voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 112. Test Condition for temperature measurement**

##### **DUT Settings**

NA

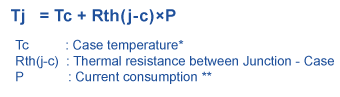
##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test device** | **Measuring Point** | **Expected operating temperature (in degree Celsius)** |
| Buck Boost(LT3790EFE) | U88 | -40°C to 125°C |

**Table 113. Requirements for temperature measurement**

##### **Test Procedure**

1. This test is conducted by configuring power supply to give a voltage of 18V.
2. Measure the case temperature on U88 using Fluke 59 Mini IR Thermometer.
3. Using the following formula calculate operating junction temperature.



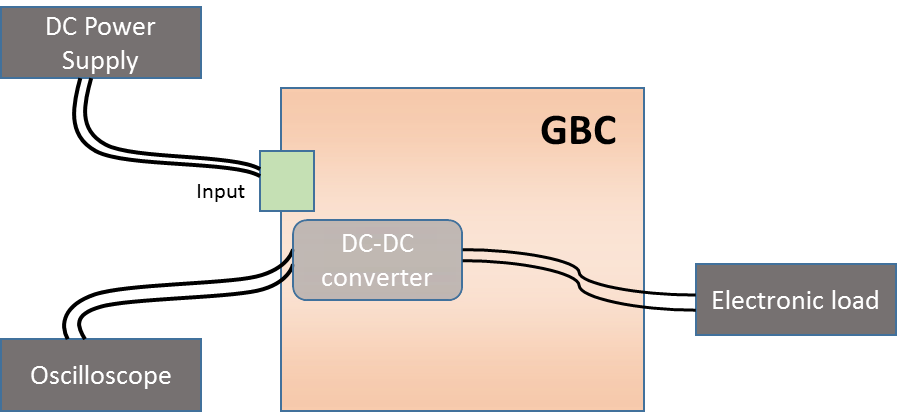
1. Ensure the derived operating junction temperature should be within the range of expected operating temperature as mentioned in the above requirement table.

##### **Reference**

Further details can be found in Page 53 of GBC schematic Ver. Life-2.

### TIVA power supply

#### Test Setup: TIVA power supply



**Figure 10. TIVA power supply - Test Setup Diagram**

#### Test Case: Ripple measurement (Test ID: PWR.7.3)

##### **Description**

1. **Purpose**The purpose of this test case is to check the maximum peak-to-peak ripple voltage of DC-DC converter output under typical load and typical input voltage condition.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | If ripple voltage is more than expected, board noise will increase and leading to failure of capacitors |
| Compliance | NA |  |

**Table 114. Impact of Failure of ripple measurement**

1. **Measurement Locations**

C502

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage scale: 20mV

1. DC power supply: E3633A

Supply Voltage: +18V DC

Current Limit: 1A

OVP: 19V

OCP: 1.5A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18VDC | Nominal voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 115. Test Condition for ripple measurement**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Voltage Rail** | **Measuring Point** | **Input Voltage(V)** | **Load current(A)** | **Maximum Ripple Voltage(mV)** |
| 3.3VD\_TIVA | C502 | 18V | Operating /Typical load | 10mVp-p |

**Table 116. Requirements for ripple measurement**

##### **Test Procedure**

1. This test is conducted by configuring power supply to give a voltage of 18V.
2. Measure ripple voltage at C502 and make sure the measured ripple voltage should be less than 10mVp-p as per the LT8640EUDC specification.

##### **Reference**

Further details can be found in Page 55 of GBC schematic Ver. Life-2.

#### Test Case: Load current measurement (Test ID: PWR.7.4)

##### **Description**

1. **Purpose**The purpose of this test case is to measure the current drawn by TIVA microcontroller when it is fully operational.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | NA |  |
| Compliance | NA |  |

**Table 117. Impact of Failure of Load current measurement**

1. **Measurement Locations**

R10054

##### **Test Equipment List**

1. DC power supply: E3633A
2. Digital multimeter: 34401A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V DC

Current Limit: 1.5A

OVP: 19V

OCP: 1.6A

1. Digital Multimeter: 34401A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18VDC | Nominal voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 118. Test Condition for Load current measurement**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |
| --- | --- | --- | --- |
| **Voltage Rail** | **Measuring Point** | **Input Voltage(V)** | **Expected Load current(A)** |
| 12V\_VIN\_TIVA | R10054 | 18V | Measured current should be equal to Current read through I2C ± 10mA |

**Table 119. Requirements for Load current measurement**

##### **Test Procedure**

1. This test is conducted by configuring power supply to give a voltage of 18V.
2. Measure voltage across sense resistor R10054 (0.002ohm).
3. Using measured voltage derive current drawn by the system.
4. Make sure the derived current should match the current read through I2C as mentioned in the above requirement table.

##### **Reference**

Further details can be found in Page 55 of GBC schematic Ver. Life-2.

#### Test Case: Temperature measurement (Test ID: PWR.7.5)

##### **Description**

1. **Purpose**The purpose of this test case is to measure the operating junction temperature of TIVA microcontroller when it is fully operational under ambient temperature.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case will result in damage of IC (U72). |
| Performance | NA |  |
| Compliance | NA |  |

**Table 120. Impact of Failure of Temperature****measurement**

1. **Measurement Locations**

U72

##### **Test Equipment List**

1. DC power supply: E3633A
2. Fluke 59 Mini IR Thermometer

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V DC

Current Limit: 2A

OVP: 19V

OCP: 2.1A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | +18V DC | Nominal voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 121. Test Condition for temperature measurement**

##### **DUT Settings**

NA

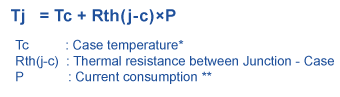
##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test device** | **Measuring Point** | **Expected operating temperature (in degree Celsius)** |
| TIVA (TM4C1294NCPDT-128-TQFP) | U72 | -40°C to 85°C |

**Table 122. Requirements for temperature measurement**

##### **Test Procedure**

1. This test is conducted by configuring power supply to give a voltage of 18V.
2. Measure the case temperature on U72 using Fluke 59 Mini IR Thermometer.
3. Using the following formula calculate operating junction temperature.



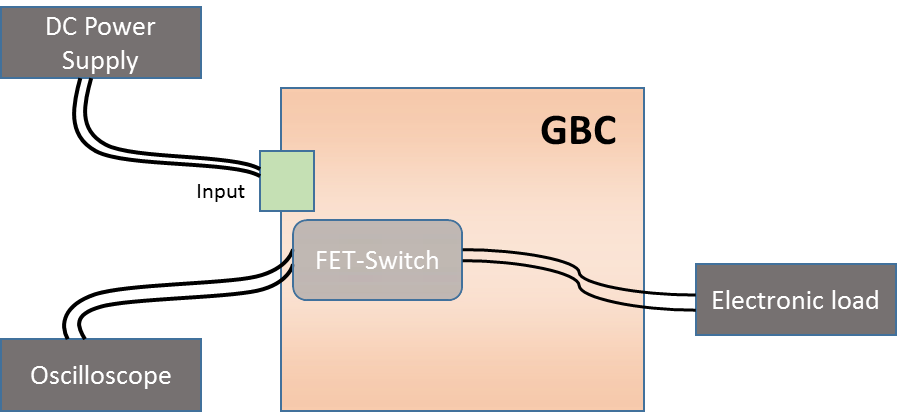
1. Ensure the derived operating junction temperature should be within the range of expected operating temperature as mentioned in the above requirement table.

##### **Reference**

Further details can be found in Page 58, 59 and 60 of GBC schematic Ver. Life-2.

### FET Switch

#### Test Setup: FET Switch



**Figure 11. FET Switch - Test Setup Diagram**

#### Test Case: Ripple measurement (Test ID: PWR.9.3)

##### **Description**

1. **Purpose**The purpose of this test case is to check the maximum peak-to-peak ripple voltage of FET switch.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | If ripple voltage is more than expected, board noise will increase and leading to failure of capacitors |
| Compliance | NA |  |

**Table 123. Impact of Failure of Ripple measurement**

1. **Measurement Locations**

C1A4

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage scale: 50mV

1. DC power supply: E3633A

Supply Voltage: +18V DC

Current Limit: 1A

OVP: 19V

OCP: 1.5A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | +18V DC | Nominal voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 124. Test Condition for Ripple measurement**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Voltage Rail** | **Measuring Point** | **Input Voltage(V)** | **Load current(A)** | **Maximum Ripple Voltage** |
| V12\_A | C1A4 | 18V | Operating load | 600mVp-p |

**Table 125. Requirements for Ripple measurement**

##### **Test Procedure**

1. This test is conducted by configuring power supply to give a voltage of 18V.
2. Measure ripple voltage at C1A4 and make sure the measured ripple voltage should be less than 600mVp-p as mentioned in the above requirement table.

##### **Reference**

Further details can be found in Page 28 and 29 of GBC schematic Ver. Life-2.

#### Test Case: Load current measurement (Test ID: PWR.9.4)

##### **Description**

1. **Purpose**The purpose of this test case is to measure the current drawn by FET switch when it is operational.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | NA |  |
| Compliance | NA |  |

**Table 126. Impact of Failure of Load current measurement**

1. **Measurement Locations**

R10067

##### **Test Equipment List**

1. DC power supply: E3633A
2. Digital multimeter: 34401A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V DC

Current Limit: 1.5A

OVP: 19V

OCP: 1.6A

1. Digital Multimeter: 34401A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18VDC | Nominal voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 127. Test Condition for Load current measurement**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |
| --- | --- | --- | --- |
| **Voltage Rail** | **Measuring Point** | **Input Voltage(V)** | **Expected Load current(A)** |
| V12\_ATOM\_IN | R10067 | 18V | Measured current should be equal to Current read through I2C ± 10mA |

**Table 128. Requirements for Load current measurement**

##### **Test Procedure**

1. This test is conducted by configuring power supply to give a voltage of 18V.
2. Measure voltage across sense resistor R10067 (0.002ohm).
3. Using measured voltage derive current drawn by the system.
4. Make sure the derived current should match the current read through I2C as mentioned in the above requirement table.

##### **Reference**

Further details can be found in Page 28 of GBC schematic Ver. Life-2.

#### Test Case: Temperature measurement (Test ID: PWR.9.5)

##### **Description**

1. **Purpose**The purpose of this test case is to measure the operating junction temperature of FET switch U248 when it is fully operational under ambient temperature.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case will result in damage of IC (U248). |
| Performance | NA |  |
| Compliance | NA |  |

**Table 129. Impact of Failure of Temperature****measurement**

1. **Measurement Locations**

U248

##### **Test Equipment List**

1. Fluke 59 Mini IR Thermometer
2. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V DC

Current Limit: 1.5A

OVP: 19V

OCP: 1.6A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | +18V DC | Nominal voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 130. Test Condition for temperature measurement**

##### **DUT Settings**

NA

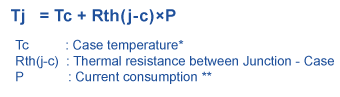
##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test device** | **Measuring Point** | **Expected operating temperature (in degree Celsius)** |
| FET (TPS259241) | U248 | -40°C to 125°C |

**Table 131. Requirements for temperature measurement**

##### **Test Procedure**

1. This test is conducted by configuring power supply to give a voltage of 18V.
2. Measure the case temperature on U248 using Fluke 59 Mini IR Thermometer.
3. Using the following formula calculate operating junction temperature.



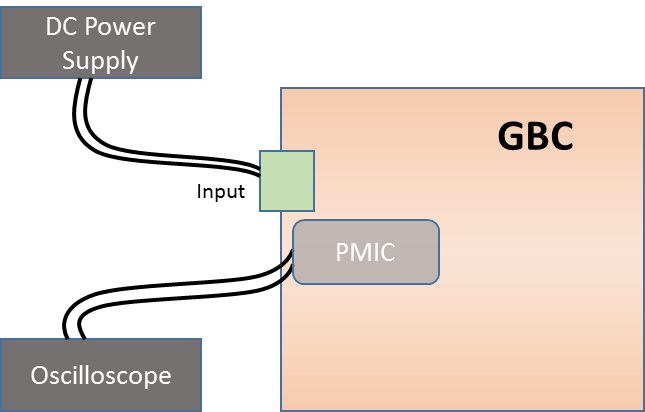
1. Ensure the derived operating junction temperature should be within the range of expected operating temperature as mentioned in the above requirement table.

##### **Reference**

Further details can be found in Page 28 of GBC schematic Ver. Life-2.

### PMIC

#### Test Setup: PMIC



**Figure 12. PMIC - Test Setup Diagram**

#### Test Case: Voltage accuracy of all output voltages (Test ID: PWR.10.2)

##### **Description**

1. **Purpose**The purpose of the test case is to measure the output voltage rails of PMIC and to ensure that these voltages are in specified limits for the proper operation of Intel SoC.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case will result in not powering the Intel and subsequent IC’s. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 132. Impact of Failure of Voltage accuracy of all output voltages**

1. **Measurement Locations**

C3M17, C4M10, C3M24, C3M8, C3M30, C3M22, C2N9, C2N11, C4P17, C1B7, C3M10, C3M11, C2B34, C2B1, C1B4, C3M180, C3M19 and C3L18

##### **Test Equipment List**

1. DC power supply: E3633A
2. Digital Multimeter

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1A

OVP: 19V

OCP: 1.1A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | +18V DC | Nominal voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 133. Test Condition for Voltage accuracy of all output voltages**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |
| --- | --- | --- | --- |
| Voltage Rail | Measuring Points | Output Voltage Specification | |
| Min(V) | Max(V) |
| V1P8\_A | C3M17 | 1.764 | 1.836 |
| VDDQ | C4M10 | 1.323 | 1.377 |
| V5\_A | C3M24 | 4.9 | 5.1 |
| V1P5\_S | C3M8 | 1.47 | 1.53 |
| VSFR\_SX | C3M30 | 1.323 | 1.377 |
| V1P35\_S | C3M22 | 1.323 | 1.377 |
| V1P2\_A | C2N9 | 1.225 | 1.275 |
| V1P2\_S | C2N11 | 1.225 | 1.275 |
| VTT\_DDR | C4P17 | 0.62775 | 0.72225 |
| V1P8\_IFSUP | C1B7 | 1.764 | 1.836 |
| VUSBPHY | C3M10 | 3.234 | 3.366 |
| V3P3\_A | C3M11 | 3.234 | 3.366 |
| VCC\_S | C2B34 | 0.98 | 1.02 |
| VNN\_S | C2B1 | 0.931 | 0.969 |
| VDDQ | C1B4 | 1.323 | 1.377 |
| V1P05\_S | C3M180 | 1.029 | 1.071 |
| V1P0\_A | C3M19 | 0.98 | 1.02 |
| V12\_A | C3L18 | 11.76 | 12.24 |

**Table 134. Requirements for Voltage accuracy of all output voltages**

##### **Test Procedure**

1. Conduct the test by configuring power supply to give a voltage of 18V.
2. Measure Voltage rails by probing at appropriate locations as mentioned in the above requirement table.
3. Make sure the measured voltages should be within the tolerance limit as mentioned in the above requirement table.

##### **Reference**

Further details can be found from Page 30 to 33 of GBC schematic Ver. Life-2.

#### Test Case: Secondary supplies enable functionality (Test ID: PWR.10.3)

##### **Description**

1. **Purpose**Purpose of the test case is to validate secondary supply rails of PMIC by checking status of dependency rails with respect to change in status (high or low).
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Dependency power rails will not enable/disable as per the requirement if this test case fails. |
| Performance | NA | . |
| Compliance | NA |  |

**Table 135. Impact of Failure of Secondary supplies enable functionality**

1. **Measurement Locations**

C3M30, C3B21, C3M30, C3B21, c3M180, C2N11, C3M8, C3M22, c3M180, C2N11, C3M8 and C3M22

##### **Test Equipment List**

1. DC power supply: E3633A
2. Oscilloscope: MSO9404A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage scale: 1V

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1A

OVP: 19V

OCP: 1.1A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | +18V DC | Nominal voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 136. Test Condition for Secondary supplies enable functionality**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Power rail | Power rail Status | Dependency rails | Measuring Points | Dependency rail status |
| PMIC\_SLP\_S0IX | High | VSFRX | C3M30 | Enable |
| V1P0SX\_EN | C3B21 | Enable |
| Low | VSFRX | C3M30 | Disable |
| V1P0SX\_EN | C3B21 | Disable |
| PMIC\_SLP\_S3 | High | V1P05\_S | c3M180 | Enable |
| V1P02\_S | C2N11 | Enable |
| V1P5\_S | C3M8 | Enable |
| V1P35\_S | C3M22 | Enable |
| Low | V1P05\_S | c3M180 | Disable |
| V1P02\_S | C2N11 | Disable |
| V1P5\_S | C3M8 | Disable |
| V1P35\_S | C3M22 | Disable |

**Table 137. Requirements for Secondary supplies enable functionality**

##### **Test Procedure**

1. Conduct the test by configuring power supply to give a voltage of 18V.
2. Validate the secondary supply rails (PMIC\_SLP\_S0IX and PMIC\_SLP\_S3) by

Measuring the dependency voltage rails status with respect to change in status of secondary supplies by probing at appropriate locations as mentioned in the above requirement table.

1. Make sure the measured voltage rails status should be as mentioned in the above requirement table.

##### **Reference**

Further details can be found in Page 33 of GBC schematic Ver. Life-2.

#### Test Case: PMIC debug circuit functionality (Test ID: PWR.10.5)

##### **Description**

1. **Purpose**The purpose of the test case is to validate debug circuit of PMIC
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Dependency power rails of debug circuit rails will not enable/disable as per the requirement if this test case fails. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 138. Impact of Failure of PMIC debug circuit functionality**

1. **Measurement Locations**

C3M30, C3B21, C3M30, C3B21, c3M180, C2N11, C3M8, C3M22, c3M180, C2N11, C3M8 and C3M22

##### **Test Equipment List**

1. DC power supply: E3633A
2. Oscilloscope: MSO9404A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage scale: 1V

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1A

OVP: 19V

OCP: 1.1A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | +18V DC | Nominal voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 139. Test Condition for PMIC debug circuit functionality**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Power rail | Power rail Status | Dependency rails | Measuring Points | Dependency rail status |
| PMIC\_SLP\_S0IX | High | VSFRX | C3M30 | Enable |
| V1P0SX\_EN | C3B21 | Enable |
| Low | VSFRX | C3M30 | Disable |
| V1P0SX\_EN | C3B21 | Disable |
| PMIC\_SLP\_S3 | High | V1P05\_S | C3M180 | Enable |
| V1P02\_S | C2N11 | Enable |
| V1P5\_S | C3M8 | Enable |
| V1P35\_S | C3M22 | Enable |
| Low | V1P05\_S | C3M180 | Disable |
| V1P02\_S | C2N11 | Disable |
| V1P5\_S | C3M8 | Disable |
| V1P35\_S | C3M22 | Disable |
| PMIC\_THERMTRIP | ­ High | All Power rails |  | Enable |
| ­ Low | All Power rails |  | Disable |

**Table 140. Requirements for PMIC debug circuit functionality**

##### **Test Procedure**

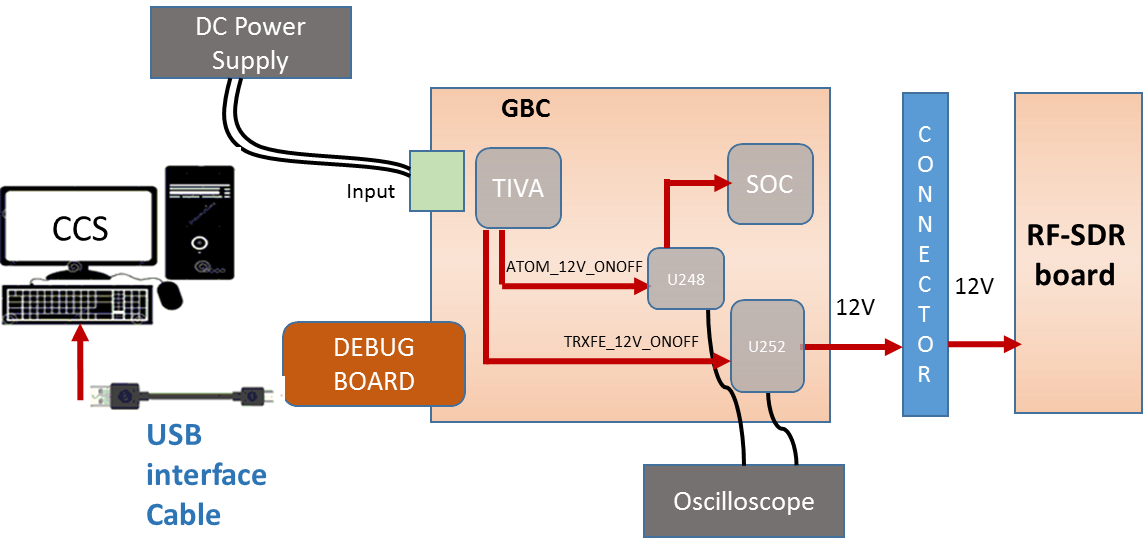
1. Conduct the test by configuring power supply to give a voltage of 18V.
2. Validate the PMIC debug circuit power rails (PMIC\_SLP\_S0IX, PMIC\_SLP\_S3 and PMIC\_THERMTRIP) by measuring dependency voltage rails status with respect to change in status of the debug power rails by probing at appropriate locations as mentioned in the above requirement table.
3. Make sure the measured voltage rails status should be as mentioned in the above requirement table.

##### **Reference**

Further details can be found in Page 33 of GBC schematic Ver. Life-2.

### System Power sequence

#### Test Setup: System Power sequence



**Figure 13. System Power sequence - Test Setup Diagram**

#### Test Case: Power-up (Test ID: PWR.11.1)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the Power-up sequence of the system including GBC and RF-SDR board.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case will result in abnormal functionality of the system. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 141. Impact of Failure of Power-up Sequence**

1. **Measurement Locations**

R10753, R10580

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 1ms

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. RF-SDR board

##### **Software Requisites**

1. Code Composer Studio Tool
2. Power Sequence code

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 142. Test Condition for Power-up Sequence**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| Sl. No | Expected sequence | Measurement Points |
| 1 | ATOM\_12V\_ONOFF | R10753 |
| 2 | TRXFE\_12V\_ONOFF | R10580 |

**Table 143. Requirements for Power-up Sequence**

##### **Test Procedure**

1. Connect Debug board to GBC board to flash the code.
2. Connect a Test PC with CCS to debug board.
3. Import the code in Code Composer Studio.
4. Run the code in CCS.
5. Configure DC power supply to give a voltage of 18V.
6. Probe the I2C signal at R10753, R10580 to measure the power up sequence of Intel Atom processor and RF-SDR board respectively.
7. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 28, 60 and 82 of GBC schematic Life-2.

#### Test Case: Power-down (Test ID: PWR.11.2)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the Power-down sequence of the system including GBC and RF-SDR board.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case will result in abnormal functionality of the system. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 144. Impact of Failure of Power-down Sequence**

1. **Measurement Locations**

R10753, R10580

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 1ms

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. RF-SDR board

##### **Software Requisites**

1. Code Composer Studio Tool
2. Power Sequence code

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 145. Test Condition for Power-down Sequence**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| Sl. No | Expected sequence | Measurement Points |
| 1 | TRXFE\_12V\_ONOFF | R10580 |
| 2 | ATOM\_12V\_ONOFF | R10753 |

**Table 146. Requirements for Power-down Sequence**

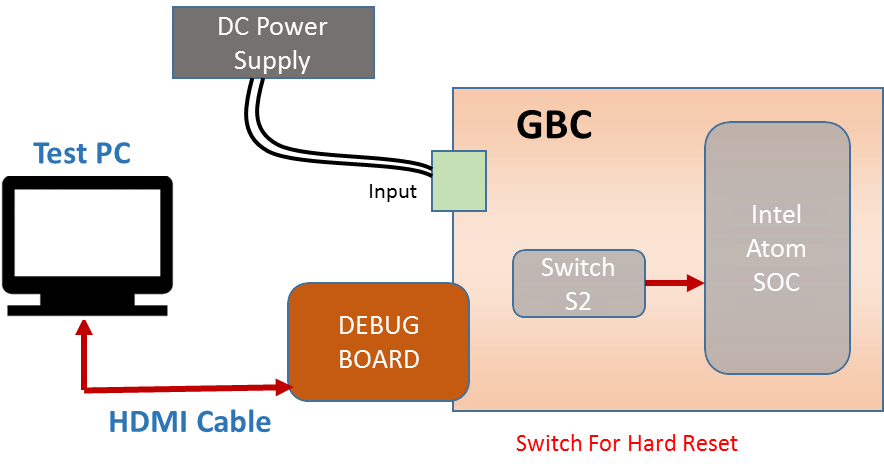
##### **Test Procedure**

1. Connect Debug board to GBC board to flash the code.
2. Connect a Test PC with CCS to debug board.
3. Import the code in Code Composer Studio.
4. Run the code in CCS.
5. Configure DC power supply to give a voltage of 18V.
6. Probe the I2C signal at R10753, R10580 to measure the power up sequence of Intel Atom processor and RF-SDR board respectively.
7. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 28, 60 and 82 of GBC schematic Life-2.

#### Test Setup: Reset



**Figure 14. Reset - Test Setup Diagram**

#### Test Case: Soft Reset (Test ID: PWR.11.3)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the soft reset for the system.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case will result in difficulty to debug on system crash or critical system failure. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 147. Impact of Failure of Soft Reset**

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

1. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 148. Test Condition for Soft Reset**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| Soft Reset | System reset | System Restarts |

**Table 149. Requirements for Soft Reset**

##### **Test Procedure**

1. Connect Debug board to GBC board with MSATA.
2. Connect a monitor to debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. After the system boots up, restart the system in Linux.

##### **Reference**

Further details can be found in Page 9 of GBC schematic Life-2.

#### Test Case: Hard Reset (Test ID: PWR.11.4)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the hard reset of the system.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case will result in difficulty to debug on system crash or critical system failure. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 150. Impact of Failure of Hard Reset**

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

1. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 151. Test Condition for Hard Reset**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| Hard Reset | System reset | System Restarts |

**Table 152. Requirements for Hard Reset**

##### **Test Procedure**

1. Connect Debug board to GBC board with MSATA.
2. Connect a monitor to debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. After the system boots up, restart the system using switch (S2).

##### **Reference**

Further details can be found in Page 77 of GBC schematic Life-2.

# CPU Sub-system

## Test Purpose and Description

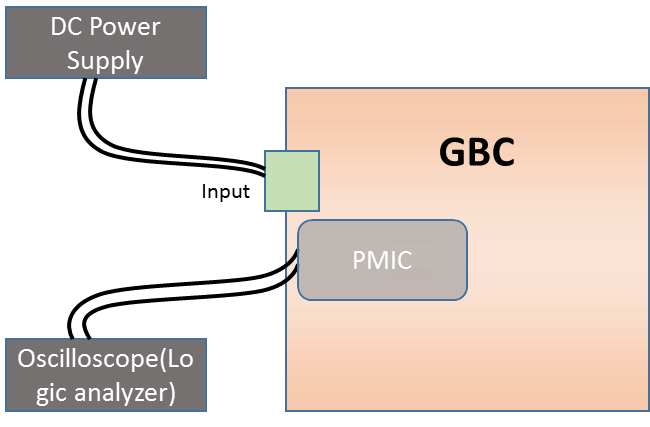
Intel ATOM E3825 is chosen as the main processor for running OpenBTS / OSMOBTS & OpenTRX SW Stack. It is having enough MIPS to be able to support processing requirements for running above mentioned SW stacks for 4 chains

## CPU Sub-system constitutes of below components

1. Intel Atom
2. PMIC - I2C
3. Springville1 – SMB
4. Springville2 – SMB
5. DDR-SMB
6. PCU – SMB
7. Springville 1 – MDI
8. TIVA- UART
9. Memory – DDR
10. Memory - SPI NOR Flash
11. Storage – mSATA
12. SpringVille1 – PCIe
13. SpringVille2- PCIe
14. TRXFE – GPIO
15. TIVA – GPIO
16. TIVA - USB 2.0
17. TRXFE- FX3 - USB 2.0
18. TRXFE- FX3 - USB 3.0
19. Debug USB 2.0
20. Debug USB 3.0
21. Debug – Ethernet
22. Display-HDMI
23. Debug-UART
24. RFSDR-PCIe

### Intel Atom

#### Test Setup



**Figure 15. Intel Atom - Test Setup Diagram**

#### Test Case: Boot configuration (Test ID: CPU.1.1)

##### **Description**

1. **Purpose**The purpose of the test case is to validate SPI NOR Flash memory by accessing the device and loading the Core Boot bios for system boot operation.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | An incorrect Bios selection or flawed manipulation, can corrupt the memory content and prevent the system from being able to reboot |
| Performance | NA |  |
| Compliance | NA |  |

**Table 153. Impact of Failure of Boot Configuration**

1. **Programming Header Location**

J16

##### **Test Equipment List**

1. SF100 ISP IC programmer
2. USB Cable
3. ISP flat cable

##### **Equipment Settings**

NA

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

CoreBoot Bios

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |
| SF100 Programmer |  | Connected to DUT and device detection |

**Table 154. Test Condition for Boot Configuration**

##### **DUT Settings**

NA

##### **Requirements**

1. Dediprog software.
2. SF100 ISP programmer and its accessories.
3. GBC Board

##### **Test Procedure**

1. Connect the programmer to the host computer via the USB cable
   1. The green LED of the programmer will be switched ON
2. The programmer is used to update directly the serial Flash on board by connecting it on the GBC ISP header / connector (J16)
   1. Ensure pin of programming header on board and color identity on the cable
3. Open the Dediprog software on the computer.
4. Click the “Detect” Icon to detect the memory on board
5. Click the “File” Icon to choose the code file
6. Click the “Prog” Icon or start button to program
   1. The SF100 programmer LED will indicate to the operator the operation on going:
   2. - Green LED ON: update successful
   3. - Orange LED: Busy in processing current execution / instruction from user
   4. - Red LED Flashing: Update failed

##### **Reference**

Further details can be found in Page 20 of GBC schematic Ver. Life-2.

#### Test Case: Power-on sequence (Test ID: CPU.1.2)

##### **Description**

1. **Purpose**The purpose of the test case is to validate sequence of PMIC power rails while powering on the system.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Functionality of the IC’s will not be in sequence as expected if this test case fails. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 155. Impact of Failure of Power-on sequence – Intel Atom**

1. **Measurement Locations**

R2B40.1, C1B7.1, C3M10, C3M19.1, C2N9.2, C3M17.1, C4M10.2, C2B34.1, C3M8.1, C3M22.1, C3B33.1

##### **Test Equipment List**

1. Oscilloscope (Logic analyzer): MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope (Logic analyzer): MSO9404A

Threshold setting: 550mV

Time scale: 100ms

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 156. Test Condition for Power-on sequence – Intel Atom**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| Power-on sequence | | |
| Expected Sequence | Measurement Points | Pass Criteria |
| PWRBTNIN | R2B40.1 | Measured sequence order should match with the expected sequence. |
| V1P8\_IFSUP | C1B7.1 |
| VUSBPHY | C3M10 |
| V1P0\_A | C3M19.1 |
| V1P2\_A | C2N9.2 |
| V1P8\_A | C3M17.1 |
| VDDQ | C4M10.2 |
| VCC | C2B34.1 |
| V1P5\_S | C3M8.1 |
| V1P35\_S | C3M22.1 |
| COREPWROK | C3B33.1 |

**Table 157. Requirements for Power-on sequence – Intel Atom**

##### **Test Procedure**

1. Configure DC power supply to give a voltage of 18V.
2. Set the trigger to PWRBTNIN (550mV).
3. While powering on the device probe power rails at appropriate locations using logic analyzer to check the sequence of power rails as mentioned in the above table.
4. Make sure the measured sequence should be as per the IDT9145-I0 specification.

##### **Reference**

Further details can be found from Page 30 to 33 of GBC schematic Ver. Life-2.

#### Test Case: Power-down Sequence (Test ID: CPU.1.3)

##### **Description**

1. **Purpose**The purpose of the test case is to validate sequence of PMIC power rails while powering off the system.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Functionality of the IC’s will not be in sequence as expected if this test case fails. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 158. Impact of Failure of Power-down sequence – Intel Atom**

1. **Measurement Locations**

R2B13.1, C3B33.1, C2B22.1, C2B34.1, C3A12.1, C2B1.1, C2N9.2, C3M17.1, C3M19.1

##### **Test Equipment List**

1. Oscilloscope (Logic analyzer): MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope (Logic analyzer): MSO9404A

Threshold setting: 550mV

Time scale: 100ms

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 159. Test Condition for Power-down sequence – Intel Atom**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| Power-down sequence | | |
| Expected sequence | Measurement Points | Pass Criteria |
| PLTRST\_B | R2B13.1 | Measured sequence order should match with the expected sequence. |
| COREPWROK | C3B33.1 |
| VDDQ\_VTT | C2B22.1 |
| VCC | C2B34.1 |
| V3P3S | C3A12.1 |
| VNN | C2B1.1 |
| V1P2\_A | C2N9.2 |
| V1P8\_A | C3M17.1 |
| V1P0\_A | C3M19.1 |

**Table 160. Requirements for Power-down sequence – Intel Atom**

##### **Test Procedure**

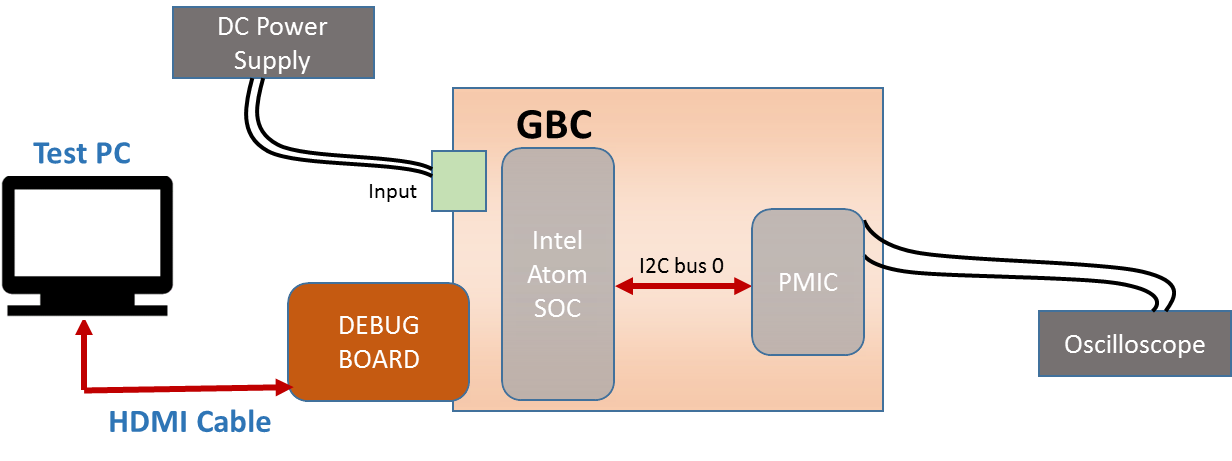
1. Configure DC power supply to give a voltage of 18V.
2. Set the trigger to PLTRST (550mV).
3. While powering off the device, probe power rails at appropriate locations using logic analyzer to check the sequence of power rails as mentioned in the above table.
4. Make sure the measured sequence should be as per the IDT9145-I0 specification.

##### **Reference**

Further details can be found from Page 30 to 33 of GBC schematic Ver. Life-2.

### PMIC – I2C (IDTP9145\_R1P15)

#### Test Setup



**Figure 16. PMIC I2C - Test Setup Diagram**

#### Test Case: Electrical Validation (Test ID: CPU.2.1)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the electrical characteristics of I2C interface between Intel Atom processor and PMIC.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | Failure of this test case will result in improper PMIC output voltages. |
| Compliance | NA |  |

**Table 161. Impact of Failure of EV – PMIC I2C**

1. **Measurement Locations**

R1B8.2, R1B14.2

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50µs

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

1. Intel Atom processor - PMIC I2C code
2. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 162. Test Condition for EV – PMIC I2C**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| SOC\_I2C\_SCL | R1B14.2 | VLOW (max) (V) | -0.5 | 0.54 |
| VHIGH (min) (V) | 1.26 | 2.3 |
| Rise time (ns) | 0 | 300 |
| Fall time (ns) | 0 | 300 |
| Frequency (kHz) | 0 | 400 |
| SOC\_I2C\_SDA | R1B8.2 | VLOW (max) (V) | -0.5 | 0.54 |
| VHIGH (min) (V) | 1.26 | 2.3 |
| Rise time (ns) | 0 | 300 |
| Fall time (ns) | 0 | 300 |

**Table 163. Requirements for EV – PMIC I2C**

##### **Test Procedure**

1. Connect Debug board to GBC board.
2. Connect a monitor to debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. Copy the code into the system after it boots up.
5. Probe the I2C signal at R1B14.2 (SCL), R1B8.2 (SDA).
6. Open the terminal and run the script.
7. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 12 and 33 of GBC schematic Life-2.

#### Test Case: Signal Integrity (Test ID: CPU.2.2)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the signal integrity of I2C interface between Intel Atom processor and PMIC.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | Failure of this test case will result in improper PMIC output voltages. |
| Compliance | NA |  |

**Table 164. Impact of Failure of SI – PMIC I2C**

1. **Measurement Locations**

R1B8.2, R1B14.2

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50µs

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

1. Intel Atom processor - PMIC I2C code
2. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 165. Test Condition for SI – PMIC I2C**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| SOC\_I2C\_SCL | R1B14.2 | Positive Over-shoot (%) | 0 | 10 |
| Negative Over-shoot (%) | 0 | 10 |
| SOC\_I2C\_SDA | R1B8.2 | Positive Over-shoot (%) | 0 | 10 |
| Negative Over-shoot (%) | 0 | 10 |
| Data set-up time (ns) | 100 | 2500 |
| Data hold time (ns) | 300 | 2500 |

**Table 166. Requirements for SI – PMIC I2C**

##### **Test Procedure**

1. Connect Debug board to GBC board.
2. Connect a monitor to debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. Copy the code into the system after it boots up.
5. Probe the I2C signal at R1B14.2 (SCL), R1B8.2 (SDA).
6. Open the terminal and run the script.
7. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 12 and 33 of GBC schematic Life-2.

#### Test Case: Functional Validation (Test ID: CPU.2.3)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the I2C interface of PMIC.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Registers of PMIC become inaccessible on failure of this test case. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 167. Impact of Failure of FV – PMIC I2C**

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

1. Intel Atom processor - PMIC I2C code
2. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 168. Test Condition for FV – PMIC I2C**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| I2C Interface | Chip revision register | Read Chip revision register, 0x05 from Address 0x01 |

**Table 169. Requirements for FV – PMIC I2C**

##### **Test Procedure**

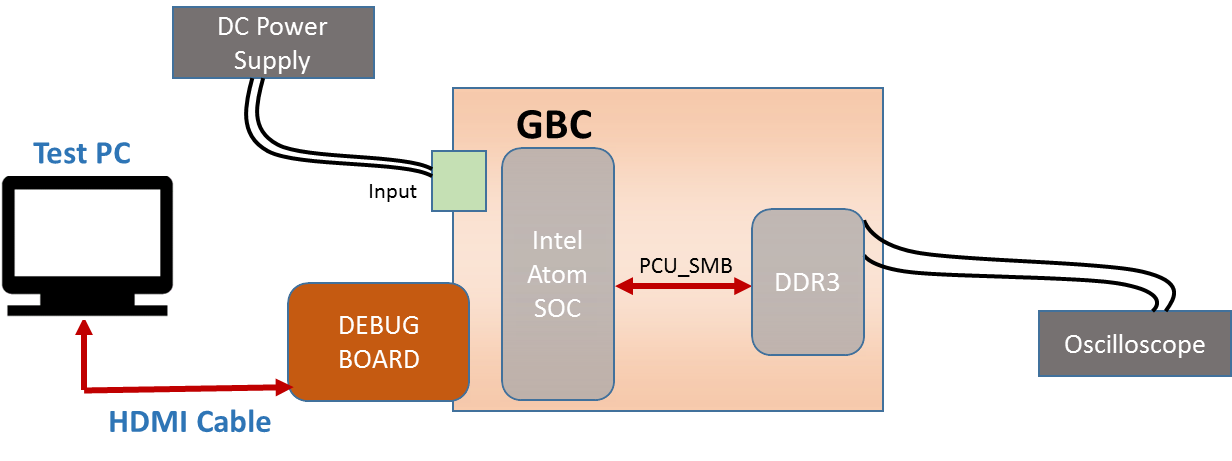
1. Connect Debug board to GBC board.
2. Connect a monitor to debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. Copy the code into the system after it boots up.
5. Open the terminal and run the script.
6. Validate the output as per the above requirement.

##### **Reference**

Further details can be found in Page 12 and 33 of GBC schematic Life-2.

### DDR - SMB (TS512MSK64W6H-I)

#### Test Setup



**Figure 17. DDR SMB- Test Setup Diagram**

#### Test Case: Electrical Validation (Test ID: CPU.5.1)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the electrical characteristics of SMBus interface between Intel Atom processor and DDR3.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | Failure of this test case will result in improper data. |
| Compliance | NA |  |

**Table 170. Impact of Failure of EV – DDR SMB**

1. **Measurement Locations**

U4D1.2, U4D1.3 and U4D1.7, U4D1.6

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50µs

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

1. Intel Atom processor – DDR3 SMB code
2. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 171. Test Condition for EV – DDR SMB**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| **Before Level Shifter** | | | | |
| PCU\_SMB\_CLK | U4D1.2 | VLOW (max) (V) | -0.5 | 0.54 |
| VHIGH (min) (V) | 1.26 | 5.5 |
| Rise time (ns) | 0 | 1000 |
| Fall time (ns) | 0 | 300 |
| Frequency (kHz) | 0 | 100 |
| PCU\_SMB\_DAT | U4D1.3 | VLOW (max) (V) | -0.5 | 0.54 |
| VHIGH (min) (V) | 1.26 | 5.5 |
| Rise time (ns) | 0 | 1000 |
| Fall time (ns) | 0 | 300 |
| **After Level Shifter** | | | | |
| SMB\_DDR3\_CLK | U4D1.7 | VLOW (max) (V) | -0.5 | 0.99 |
| VHIGH (min) (V) | 2.31 | 3.8 |
| Rise time (ns) | 0 | 1000 |
| Fall time (ns) | 0 | 300 |
| Frequency (kHz) | 0 | 100 |
| SMB\_DDR3\_DAT | U4D1.6 | VLOW (max) (V) | -0.5 | 0.99 |
| VHIGH (min) (V) | 2.31 | 3.8 |
| Rise time (ns) | 0 | 1000 |
| Fall time (ns) | 0 | 300 |

**Table 172. Requirements for EV – DDR SMB**

##### **Test Procedure**

1. Connect Debug board to GBC board.
2. Connect a monitor to debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. Copy the code into the system after it boots up.
5. Probe the I2C signal at U4D1.2 (SCLK), U4D1.3 (SDATA) for before level shifter and U4D1.7 (SCLK), U4D1.6 (SDATA) for after level shifter respectively.
6. Open the terminal and run the script.
7. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 12, 15 and 16 of GBC schematic Life-2.

#### Test Case: Signal Integrity (Test ID: CPU.5.2)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the signal integrity of SMBus interface between Intel Atom processor and DDR3.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA | . |
| Performance | Yes | Failure of this test case will result in improper data. |
| Compliance | NA |  |

**Table 173. Impact of Failure of SI – DDR SMB**

1. **Measurement Locations**

U4D1.2, U4D1.3 and U4D1.7, U4D1.6

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50µs

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

1. Intel Atom processor – DDR3 SMB code
2. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 174. Test Condition for SI – DDR SMB**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| **Before Level Shifter** | | | | |
| PCU\_SMB\_CLK | U4D1.2 | Positive Over-shoot (V) | 0 | 0.18 |
| Negative Over-shoot (V) | 0 | 0.18 |
| PCU\_SMB\_DAT | U4D1.3 | data set-up time (ns) | 250 | 10000 |
| data hold time (ns) | 300 | 10000 |
| Positive Over-shoot (V) | 0 | 0.18 |
| Negative Over-shoot (V) | 0 | 0.18 |
| **After Level Shifter** | | | | |
| SMB\_DDR3\_CLK | U4D1.7 | Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |
| SMB\_DDR3\_DAT | U4D1.6 | data set-up time (ns) | 250 | 10000 |
| data hold time (ns) | 300 | 10000 |
| Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |

**Table 175. Requirements for SI – DDR SMB**

##### **Test Procedure**

1. Connect Debug board to GBC board.
2. Connect a monitor to debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. Copy the code into the system after it boots up.
5. Probe the I2C signal at U4D1.2 (SCLK), U4D1.3 (SDATA) for before level shifter and U4D1.7 (SCLK), U4D1.6 (SDATA) for after level shifter respectively.
6. Open the terminal and run the script.
7. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 12, 15 and 16 of GBC schematic Life-2.

#### Test Case: Functional Validation (Test ID: CPU.5.3)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the SMBus interface of DDR.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Registers of DDR become inaccessible on failure of this test case. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 176. Impact of Failure of FV – DDR SMB**

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

1. Intel Atom processor – DDR3 SMB code
2. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 177. Test Condition for FV – DDR SMB**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| I2C Interface | Device register address | Read device register address from 128 to 145 |

**Table 178. Requirements for FV – DDR SMB**

##### **Test Procedure**

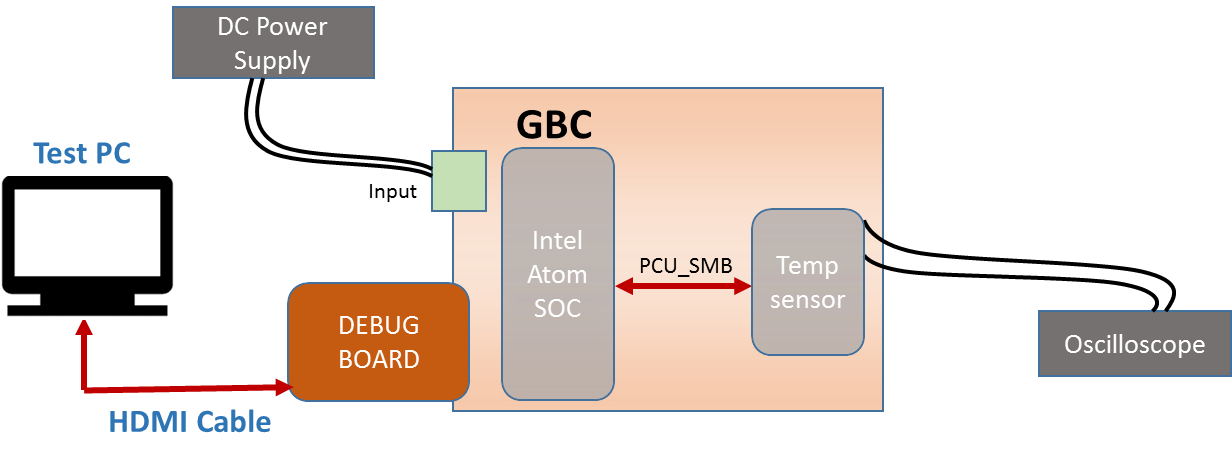
1. Connect Debug board to GBC board.
2. Connect a monitor to debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. Copy the code into the system after it boots up.
5. Open the terminal and run the script.
6. Validate the output as per the above requirement.

##### **Reference**

Further details can be found in Page 12, 15 and 16 of GBC schematic Life-2.

### PCU – SMB (ADT7481)

#### Test Setup



**Figure 18. PCU SMB- Test Setup Diagram**

#### Test Case: Electrical Validation (Test ID: CPU.6.1)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the electrical characteristics of SMBus interface between Intel Atom processor and temperature sensor.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | Failure of this test case will result in improper temperature readings. |
| Compliance | NA |  |

**Table 179. Impact of Failure of EV – PCU SMB**

1. **Measurement Locations**

U2A1.2, U2A1.3 and U3A1.10, U3A1.9

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50µs

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

1. Intel Atom processor – Temp sensor SMB code
2. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 180. Test Condition for EV – PCU SMB**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| **Before Level Shifter** | | | | |
| PCU3\_SMB\_CLK | U2A1.2 | VLOW (max) (V) | -0.5 | 0.54 |
| VHIGH (min) (V) | 1.26 | 5.5 |
| Rise time (ns) | 0 | 1000 |
| Fall time (ns) | 0 | 300 |
| Frequency (kHz) | 0 | 100 |
| PCU3\_SMB\_DAT | U2A1.3 | VLOW (max) (V) | -0.5 | 0.54 |
| VHIGH (min) (V) | 1.26 | 5.5 |
| Rise time (ns) | 0 | 1000 |
| Fall time (ns) | 0 | 300 |
| **After Level Shifter** | | | | |
| SMB\_3P3\_CLK | U3A1.10 | VLOW (max) (V) | -0.5 | 0.8 |
| VHIGH (min) (V) | 2.1 | 3.8 |
| Rise time (ns) | 0 | 1000 |
| Fall time (ns) | 0 | 300 |
| Frequency (kHz) | 0 | 100 |
| SMB\_3P3\_DAT | U3A1.9 | VLOW (max) (V) | -0.5 | 0.8 |
| VHIGH (min) (V) | 2.1 | 3.8 |
| Rise time (ns) | 0 | 1000 |
| Fall time (ns) | 0 | 300 |

**Table 181. Requirements for EV – PCU SMB**

##### **Test Procedure**

1. Connect Debug board to GBC board.
2. Connect a monitor to debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. Copy the code into the system after it boots up.
5. Probe the I2C signal at U2A1.2 (SCLK), U2A1.3 (SDATA) for before level shifter and U3A1.10 (SCLK), U3A1.9 (SDATA) for after level shifter respectively.
6. Open the terminal and run the script.
7. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 12, 15 and 38 of GBC schematic Life-2.

#### Test Case: Signal Integrity (Test ID: CPU.6.2)

##### **Description**

1. **Purpose**

The purpose of the test case is to validate the signal integrity of SMBus interface between Intel Atom processor and temperature sensor.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | Failure of this test case will result in improper temperature readings. |
| Compliance | NA |  |

**Table 182. Impact of Failure of SI – PCU SMB**

1. **Measurement Locations**

U2A1.2, U2A1.3 and U3A1.10, U3A1.9

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50µs

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

1. Intel Atom processor – Temp sensor SMB code
2. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 183. Test Condition for SI – PCU SMB**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| **Before Level Shifter** | | | | |
| PCU3\_SMB\_CLK | U2A1.2 | Positive Over-shoot (V) | 0 | 0.18 |
| Negative Over-shoot (V) | 0 | 0.18 |
| PCU3\_SMB\_DAT | U2A1.3 | data set-up time (ns) | 250 | 10000 |
| data hold time (ns) | 300 | 10000 |
| Positive Over-shoot (V) | 0 | 0.18 |
| Negative Over-shoot (V) | 0 | 0.18 |
| **After Level Shifter** | | | | |
| SMB\_3P3\_CLK | U3A1.10 | Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |
| SMB\_3P3\_DAT | U3A1.9 | data set-up time (ns) | 250 | 10000 |
| data hold time (ns) | 300 | 10000 |
| Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |

**Table 184. Requirements for SI – PCU SMB**

##### **Test Procedure**

1. Connect Debug board to GBC board.
2. Connect a monitor to debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. Copy the code into the system after it boots up.
5. Probe the I2C signal at U2A1.2 (SCLK), U2A1.3 (SDATA) for before level shifter and U3A1.10 (SCLK), U3A1.9 (SDATA) for after level shifter respectively.
6. Open the terminal and run the script.
7. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 12, 15 and 38 of GBC schematic Life-2.

#### Test Case: Functional Validation (Test ID: CPU.6.3)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the SMBus interface of temperature sensor.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Registers of the temperature sensor become inaccessible on failure of this test case. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 185. Impact of Failure of FV – PCU SMB**

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

1. Intel Atom processor – Temp sensor SMB code
2. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 186. Test Condition for FV – PCU SMB**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| I2C Interface | Device ID | Read Device ID, 0x81 from Address 0x3D |
| Manufacturer ID | Read Manufacturer ID, 0x41 from Address 0x3E |

**Table 187. Requirements for FV – PCU SMB**

##### **Test Procedure**

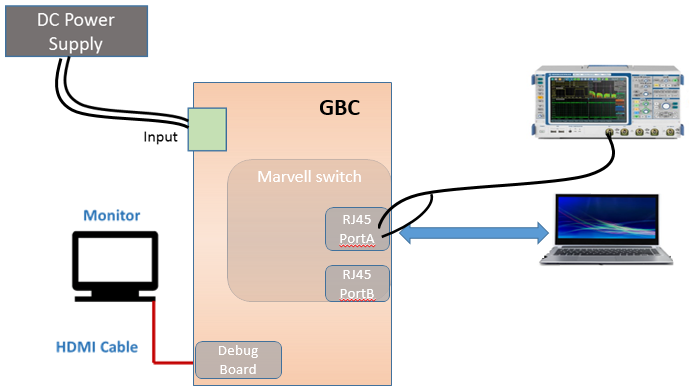
1. Connect Debug board to GBC board.
2. Connect a monitor to debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. Copy the code into the system after it boots up.
5. Open the terminal and run the script.
6. Validate the output as per the above requirement.

##### **Reference**

Further details can be found in Page 12, 15 and 38 of GBC schematic Life-2.

### Springville 1 – MDI

#### Test Setup



**Figure 19.INTEL Springville 1 MDI - Test Setup Diagram**

#### Test Case: Signal characteristics (Test ID: CPU.7.1)

##### **Description**

1. **Purpose**The purpose of this test case is to verify MDI signal characteristics (Interface between Marvell Switch (88E6071) to Springville PHY (WGI210AT)
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Packet loss and data inconsistency |
| Performance | Yes | Improper data transfer and loss of data |
| Compliance | NA |  |

**Table 188. Impact of Failure of SI – Springville 1 MDI**

1. **Measurement Locations**

R962.2, R963.2, L1M2.6, L1M2.8

##### **Test Equipment List**

1. Oscilloscope: DPO7354C
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: DPO7354C

Voltage per division: 500mV

Time scale: 50ns

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. HDMI Monitor

##### **Software Requisites**

1. Ethernet driver
2. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 189. Test Condition for SI – Springville 1 MDI**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| **MDIO – TX (**From Springville to Switch) | | | | |
| MDI0P  MDI0N | R962.2  R963.2 | Vp-p (V) | 0.95 | 1.05 |
| Overshoot (%) | 0 | 5 |
| Undershoot (%) | 0 | 5 |
| Data rate (Mbps) |  | 100 |
| **MDIO – RX (**From Switch to Springville) | | | | |
| LAN\_MDI1P  LAN\_MDI1N | L1M2.6  L1M2.8 | Vp-p (V) | 0.95 | 1.05 |
| Overshoot (%) | 0 | 5 |
| Undershoot (%) | 0 | 5 |
| Data rate (Mbps) |  | 100 |

**Table 190. Requirements for SI – Springville 1 MDI**

##### **Test Procedure**

1. Connect Debug board to GBC board with OS and Ethernet driver installed
2. Connect a monitor to debug board using HDMI cable
3. Connect a Linux PC to port A of GBC board.
4. Configure DC power supply to give a voltage of 18V.
5. Assign static IP address at both GBC and Linux PC.
6. Establish communication by pinging each other.
7. The MDI transmit signals (from Springville to Switch) are measured at R962.2 (MDI0P) and R963.2 (MDI0N).
8. The MDI receiving signals (from Switch to Springville) are measured at L1M2.6 (MDI1P) and L1M2.8 (MDI1N).
9. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 23, 24 and 60 of GBC schematic Life-2.

#### Test Case: Functional Validation (Test ID: CPU.7.2)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the function of springville1-MDI.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Registers of SOC become inaccessible on failure of this test case and data transfer can be affected. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 191. Impact of Failure of FV – Springville 1 MDI**

##### **Test Equipment List**

1. Oscilloscope: DPO7354C
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: DPO7354C

Voltage per division: 500mV

Time scale: 50ns

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. HDMI Monitor

##### **Software Requisites**

1. Ethernet driver
2. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 192. Test Condition of FV – Springville 1 MDI**

##### **DUT Settings**

NA.

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| Ethernet Interface | IP Address | Ping each other using static IP address and ensure the data transfer with no packet loss |

**Table 193. Requirements for FV – Springville 1 MDI**

##### **Test Procedure**

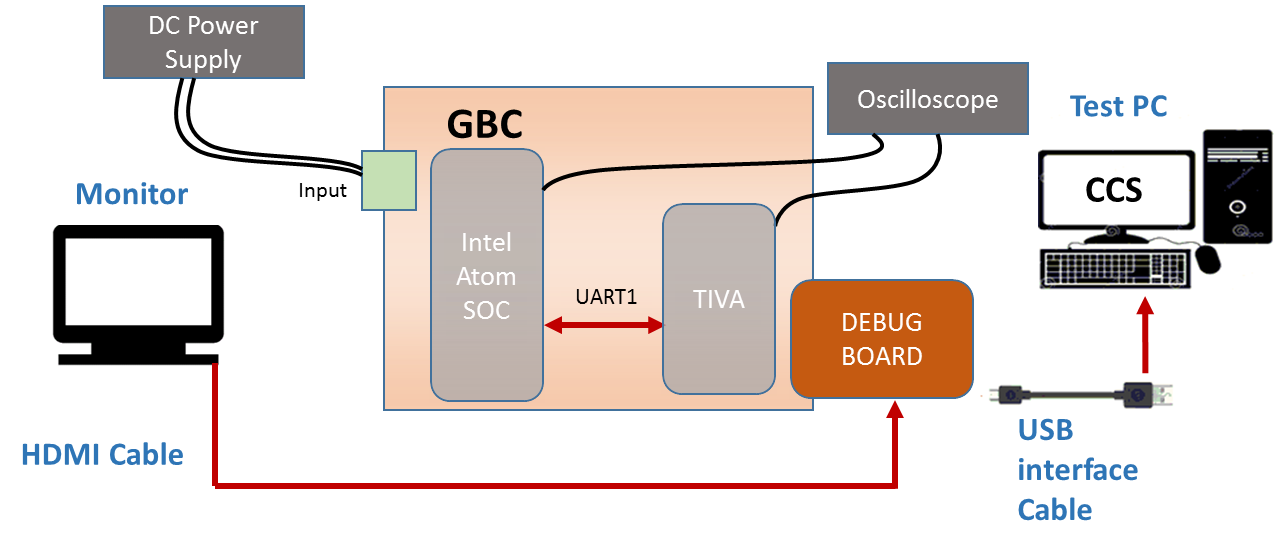
1. Connect Debug board to GBC board with OS and Ethernet driver installed
2. Connect a monitor to debug board using HDMI cable
3. Connect a Linux PC to port A of GBC board.
4. Configure DC power supply to give a voltage of 18V.
5. Assign static IP address at both GBC and Linux PC.
6. Establish communication by pinging each other.
7. Validate the output as per the above requirement.

##### **Reference**

Further details can be found in Page 23, 24 and 60 of GBC schematic Life-2.

### TIVA - UART

#### Test Setup



**Figure 20.TIVA UART- Test Setup Diagram**

#### Test Case: Signal characteristics (Test ID: CPU.8.1)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the electrical characteristics of UART interface between Tiva controller and Intel Atom processor.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | Improper data transfer between SOC and TIVA |
| Compliance | NA |  |

**Table 194. Impact of Failure of SI – TIVA UART**

1. **Measurement Locations**

R10550, R10472

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 10µs

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

1. Code Composer Studio Tool
2. Tiva - Intel UART code
3. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 195. Test Condition for SI – TIVA UART**

##### **DUT Settings**

Resistor R10511 is removed and Pin 2 of the resistor is connected to ground to enable the level shifter.

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| **UART TX** | | | | |
| ISO\_TIVA\_SOC\_UART3\_TX | R10550 | VLOW (V) | -0.378 | 0.63 |
| VHIGH (V) | 1.17 | 2.232 |
| Positive Overshoot (V) | 0 | 0.18 |
| Negative Overshoot (V) | 0 | 0.18 |
| **UART RX** | | | | |
| TIVA\_SOC\_UART3\_RX | R10472 | VLOW (V) | 0 | 1.155 |
| VHIGH (V) | 2.145 | 4 |
| Positive Overshoot (V) | 0 | 0.33 |
| Negative Overshoot (V) | 0 | 0.33 |

**Table 196. Requirements for SI – TIVA UART**

##### **Test Procedure**

1. Connect Debug board to GBC board.
2. Connect a Test PC with CCS to debug board.
3. Import the code in Code Composer Studio.
4. Connect a monitor to debug board using HDMI cable.
5. Configure DC power supply to give a voltage of 18V.
6. Probe the UART TX signal at R10550 and UART RX signal at R10472.
7. Program TIVA firmware.
8. Load and run the middleware in Intel SOC to request any status (Temperature, current) from TIVA and receive data on Console (SOC) through UART interface.
9. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 9, 60 and 83 of GBC schematic Life-2.

#### Test Case: Functional Validation (Test ID: CPU.8.2)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the function of UART interface between Tiva controller and Intel Atom processor.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Registers of TIVA / SOC become inaccessible on failure of this test case and data transfer can be affected. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 197. Impact of Failure of FV – TIVA UART**

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

1. Code Composer Studio Tool
2. Tiva- Intel UART code
3. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 198. Test Condition for FV – TIVA UART**

##### **DUT Settings**

Resistor R10511 is removed and Pin 2 of the resistor is connected to ground to enable the level shifter.

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| UART Interface | Intel temperature Reading | Send message from SOC to TIVA to request the temperature and get the response from TIVA. |

**Table 199. Requirements for FV – TIVA UART**

##### **Test Procedure**

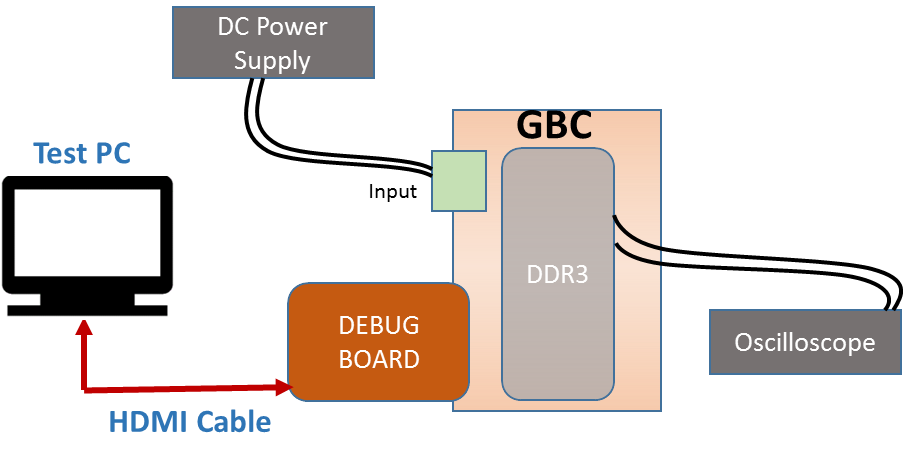
1. Connect Debug board to GBC board.
2. Connect a Test PC with CCS to debug board.
3. Import the code in Code Composer Studio.
4. Connect a monitor to debug board using HDMI cable.
5. Configure DC power supply to give a voltage of 18V.
6. Program TIVA firmware.
7. Load and run the middleware in Intel SOC to request any status (Temperature, current) from TIVA and receive data on Console (SOC) through UART interface.
8. Validate the output as per the above requirement.

##### **Reference**

Further details can be found in Page 9, 60 and 83 of GBC schematic Life-2.

### Memory - DDR

#### Test Setup

  
**NOTE:**

1. For Reference voltage measurement, Test PC not required
2. For Schmoo test, GBC board has to be put in thermal chamber.

**Figure 21. Memory DDR - Test Setup Diagram**

#### Test Case: Reference voltage measurement (Test ID: CPU.9.1)

##### **Description**

1. **Purpose**The purpose of the test case is to measure the reference voltages of DDR (DDR\_VREF and DDR\_VTT).
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case may cause the referencing signals never to trigger or to trigger prematurely. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 200. Impact of Failure of Reference voltage measurement – Memory DDR**

1. **Measurement Locations**

R2P7.1/R3P12.1, C4P17.1, C3P14.1

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 10ns

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 201. Test Condition for Reference voltage measurement – Memory DDR**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Sl. No. | Test | Probing Point | Expected Voltage(V) | Specification | |
| Min(V) | Max(V) |
| 1 | VDDQ | C3P14.1 | 1.35 | 1.28 | 1.45 |
| 2 | VREF/DQ | R2P7.1 | 0.675 | 0.64 | 0.725 |
| 3 | VREFCA | R3P12.1 | 0.675 | 0.64 | 0.725 |
| 4 | VTT\_DDR | C4P17.1 | 0.675 | 0.64 | 0.725 |

**Table 202. Requirements for Reference voltage measurement – Memory DDR**

##### **Test Procedure**

1. Configure DC power supply to give a voltage of 18V.
2. Measure the voltages on GBC board at C3P14.1, R2P7.1, R3P12.1, and C4P17.1.
3. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 17 GBC schematic Life-2.

#### Test Case: Schmoo Test (Test ID: CPU.9.2)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the DDR module by varying VREF voltage within the limits at different temperatures.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case can result in improper functioning of DDR in the specified temperature or Vref voltage. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 203. Impact of Failure of Schmoo Test – Memory DDR**

1. **Measurement Locations**

R2P7, C3P14

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 1µs

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

1. OS loaded MSATA
2. memtester utility

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 204. Test Condition for Schmoo Test – Memory DDR**

##### **DUT Settings**

R2P7, R3P12, R2P11, R3P6 values should be changed according to below mentioned requirements.

##### **Requirements**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Memory - DDR VREF measurement** | | | | | | | | | |
| Sl. No. | Probing Point | | Temperature Condition (°C) | Resistor Value (kΩ) - R2P7/R3P12 | | Resistor Value (kΩ) - R2P11/R3P6 | Expected Voltage (V) | Specification | |
| Min(V) | Max(V) |
| 1 | R2P7 | | -20 | 4.42 | | 4.7 | 0.654 | 0.64 | 0.725 |
| 2 | 0 | 4.42 | | 4.7 | 0.654 | 0.64 | 0.725 |
| 3 | 20 | 4.42 | | 4.7 | 0.654 | 0.64 | 0.725 |
| 4 | 25 | 4.42 | | 4.75 | 0.651 | 0.64 | 0.725 |
| 5 | 40 | 4.42 | | 4.7 | 0.654 | 0.64 | 0.725 |
| 6 | 70 | 4.42 | | 4.7 | 0.654 | 0.64 | 0.725 |
| 7 | -20 | 4.99 | | 4.7 | 0.695 | 0.64 | 0.725 |
| 8 | 0 | 4.99 | | 4.7 | 0.695 | 0.64 | 0.725 |
| 9 | 20 | 4.99 | | 4.7 | 0.695 | 0.64 | 0.725 |
| 10 | 25 | 4.99 | | 4.7 | 0.695 | 0.64 | 0.725 |
| 11 | 40 | 4.99 | | 4.7 | 0.695 | 0.64 | 0.725 |
| 12 | 70 | 4.99 | | 4.7 | 0.695 | 0.64 | 0.725 |
| 13 | -20 | 5.11 | | 4.42 | 0.724 | 0.64 | 0.725 |
| 14 | 0 | 5.11 | | 4.42 | 0.724 | 0.64 | 0.725 |
| 15 | 20 | 5.11 | | 4.42 | 0.724 | 0.64 | 0.725 |
| 16 | 25 | 5.11 | | 4.42 | 0.724 | 0.64 | 0.725 |
| 17 | 40 | 5.11 | | 4.42 | 0.724 | 0.64 | 0.725 |
| 18 | 70 | 5.11 | | 4.42 | 0.724 | 0.64 | 0.725 |
| **Memory - DDR VDDQ measurement** | | | | | | | | | |
| Sl. No. | Probing Point | Temperature Condition (°C) | | | Resistor Value (kΩ) - R2P7/R3P12 | Resistor Value (kΩ) - R2P11/R3P6 | Expected Voltage (V) | Specification | |
| Min(V) | Max(V) |
| 1 | C3P14 | -20 | | | 4.42 | 4.7 | 1.35 | 1.28 | 1.45 |
| 2 | 0 | | | 4.42 | 4.7 | 1.35 | 1.28 | 1.45 |
| 3 | 20 | | | 4.42 | 4.7 | 1.35 | 1.28 | 1.45 |
| 4 | 25 | | | 4.42 | 4.75 | 1.35 | 1.28 | 1.45 |
| 5 | 40 | | | 4.42 | 4.7 | 1.35 | 1.28 | 1.45 |
| 6 | 70 | | | 4.42 | 4.7 | 1.35 | 1.28 | 1.45 |
| 7 | -20 | | | 4.99 | 4.7 | 1.35 | 1.28 | 1.45 |
| 8 | 0 | | | 4.99 | 4.7 | 1.35 | 1.28 | 1.45 |
| 9 | 20 | | | 4.99 | 4.7 | 1.35 | 1.28 | 1.45 |
| 10 | 25 | | | 4.99 | 4.7 | 1.35 | 1.28 | 1.45 |
| 11 | 40 | | | 4.99 | 4.7 | 1.35 | 1.28 | 1.45 |
| 12 | 70 | | | 4.99 | 4.7 | 1.35 | 1.28 | 1.45 |
| 13 | -20 | | | 5.11 | 4.42 | 1.35 | 1.28 | 1.45 |
| 14 | 0 | | | 5.11 | 4.42 | 1.35 | 1.28 | 1.45 |
| 15 | 20 | | | 5.11 | 4.42 | 1.35 | 1.28 | 1.45 |
| 16 | 25 | | | 5.11 | 4.42 | 1.35 | 1.28 | 1.45 |
| 17 | 40 | | | 5.11 | 4.42 | 1.35 | 1.28 | 1.45 |
| 18 | 70 | | | 5.11 | 4.42 | 1.35 | 1.28 | 1.45 |

**Table 205. Requirements for Schmoo Test – Memory DDR**

##### **Test Procedure**

1. Connect Debug board to GBC board.
2. Connect a monitor to debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. Measure the voltages at R2P7, C3P14.
5. Open the terminal and execute ‘memtester’ utility on SoC for different voltages of DDR\_VREF at different temperatures.
6. DDR\_VREF can be varied by changing the voltage divide resistors, R2P11, R2P7, R3P6 and R3P12 such that there can be three co-ordinates within the specified range of DDR module.
7. In each co-ordinate, memtester utility is executed at six different temperatures to validate VREF Schmoo.
8. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 17 GBC schematic Life-2.

#### Test Case: Functional Validation (Test ID: CPU.9.3)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the entire DDR memory using memtest option at boot stage.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case can result the DDR to   1. Not accept and correctly retain arbitrary patterns of data written to it. 2. Cause errors where different bits of memory interact. 3. Cause conflicts between memory addresses. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 206. Impact of Failure of FV – Memory DDR**

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

1. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 207. Test Condition for FV – Memory DDR**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| Memory DDR | Memtest function | Results of memtest are captured to check for any errors. |

**Table 208. Requirements for FV – Memory DDR**

##### **Test Procedure**

1. Connect Debug board to GBC board.
2. Connect a monitor to debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. Execute memtest function during boot stage.
5. Validate the output as per the above requirement.

##### **Reference**

Further details can be found in Page 17 GBC schematic Life-2.

#### Test Case: Throughput measurement (Test ID: CPU.9.4)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the DDR memory for its latency and bandwidth.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | System requirement will not be met in case of failure of this test case. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 209. Impact of Failure of Throughput measurement** **– Memory DDR**

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

1. OS loaded MSATA with lmbench 3.0

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 210. Test Condition for Throughput measurement – Memory DDR**

##### **DUT Settings**

NA

##### **Test Procedure**

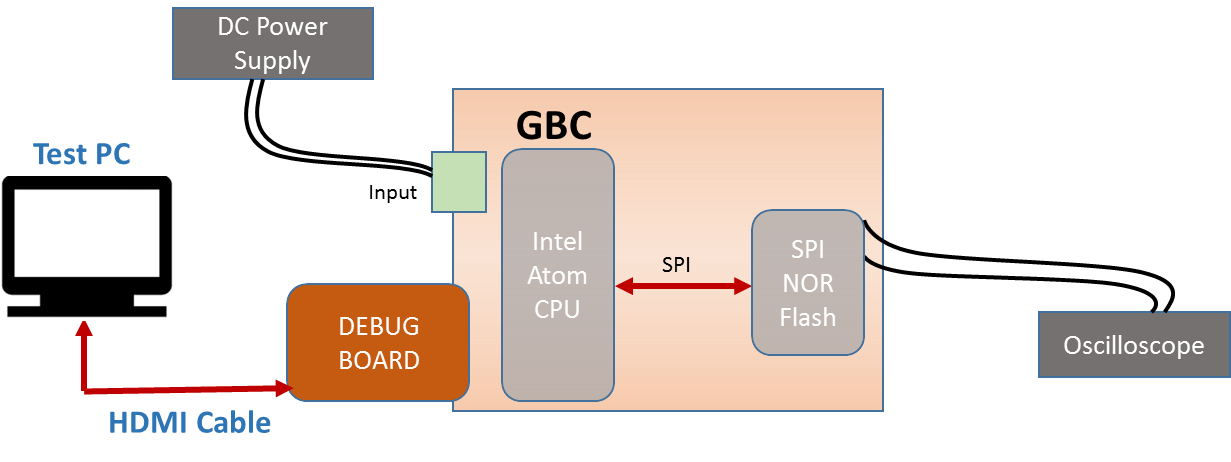
1. Connect Debug board to GBC board.
2. Connect a monitor to debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. Lmbench 3.0 is a suite of simple, portable, ANSI/C micro benchmarks for UNIX/POSIX used for throughput measurement.
5. Download the source code in to the target machine.
6. Unpack the source code.
7. Go to the original directory and run “make results see”.exe.
8. The results will be saved in lmbench directory.
9. Read / Write throughputs which are read in Mbps data speed which are there in the last result columns along with other tests results. Latencies for read / writes are also mentioned in nSec or suitable units.

##### **Reference**

Further details can be found in Page 17 GBC schematic Life-2.

### Memory SPI NOR Flash

#### Test Setup



**Figure 22. Memory SPI NOR Flash - Test Setup Diagram**

#### Test Case: Electrical Validation (Test ID: CPU.10.1)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the electrical characteristics of SPI interface of SPI NOR Flash.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | The failure of this test case will results not booting the system up. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 211. Impact of Failure of EV – Memory SPI NOR Flash**

1. **Measurement Locations**

R10762.2, R1M11.2

##### **Test Equipment List**

1. Oscilloscope: DPO7354C
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: DPO7354C

Voltage per division: 1V

Time scale: 50µs

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

1. Core boot

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 212. Test Condition for EV – Memory SPI NOR Flash**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Observation | Specification | |
| Min | Max |
| SOC\_FLASH\_CLK | R10762.2 | VLOW (max) (V) | -4.47e-13 | -0.5 | 0.54 |
| VHIGH (min) (V) | 1.64 | 1.26 | 2.2 |
| Rise time (V/ns) | 0.1906 | 0.1 | 3 |
| Fall time (V/ns) | 0.1682 | 0.1 | 3 |
| Frequency (MHz) | 33.33 | 0 | 50 |
| SOC\_SPI\_MISO | R1M11.2 | VLOW (max) (V) | 0.02 | -0.5 | 0.54 |
| VHIGH (min) (V) | 1.82 | 1.26 | 2.2 |
| Rise time (V/ns) | 0.2028 | 0.1 | 3 |
| Fall time (V/ns) | 0.2025 | 0.1 | 3 |

**Table 213. Requirements for EV – Memory SPI NOR Flash**

##### **Test Procedure**

1. Connect Debug board to GBC board.
2. Connect a monitor to Debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. Flash the core boot into SPI NOR FLASH.
5. While system booting probe the SPI signals at R10762. (SOC\_FLASH\_CLK), R1M11.2 (SOC\_SPI\_MISO).
6. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 20 and 9 of GBC schematic Ver. Life-2.

#### Test Case: Signal Integrity (Test ID: CPU.10.2)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the signal integrity of SPI interface of SPI NOR Flash.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | The failure of this test case will results not booting the system up. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 214. Impact of Failure of SI – Memory - SPI NOR Flash**

1. **Measurement Locations**

R10762.2, R1M11.2

##### **Test Equipment List**

1. Oscilloscope: DPO7354C
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: DPO7354C

Voltage per division: 1V

Time scale: 50µs

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

1. Core boot

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 215. Test Condition for SI – Memory - SPI NOR Flash**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| SOC\_FLASH\_CLK | R10762 | Positive Over-shoot (V) | 0 | 0.18 |
| Negative Over-shoot (V) | 0 | 0.18 |
| SOC\_SPI\_MISO | R1M11.2 | Positive Over-shoot (V) | 0 | 0.18 |
| Negative Over-shoot (V) | 0 | 0.18 |
| data set-up time (ns) | 2 | 100 |
| data hold time (ns) | 3 | 100 |

**Table 216. Requirements for SI – Memory - SPI NOR Flash**

##### **Test Procedure**

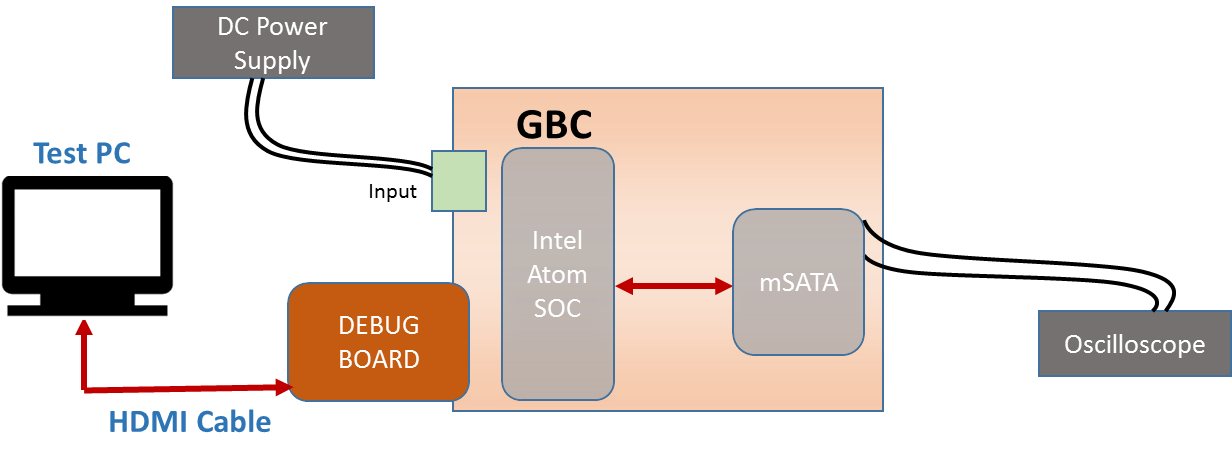
1. Connect Debug board to GBC board.
2. Connect a monitor to Debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. Flash the core boot into SPI NOR FLASH.
5. While system booting probe the SPI signals at R10762. (SOC\_FLASH\_CLK), R1M11.2 (SOC\_SPI\_MISO).
6. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 20 and 9 of GBC schematic Ver. Life-2.

### Storage - mSATA

#### Test Setup



**NOTE:**

1. Monitor required only for I/O Stress.
2. Oscilloscope required only for Signal Integrity.

**Figure 23. Storage mSATA- Test Setup Diagram**

#### Test Case: Signal integrity (Test ID: CPU.11.1)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the signal integrity of mSATA signals by plotting the eye diagram.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | Failure of this test case can result in errors in the OS loaded in mSATA. |
| Compliance | NA |  |

**Table 217. Impact of Failure of SI – Storage mSATA**

1. **Measurement Locations**

C1833.1 and C1834.1, C1835.2 and C1836.2

##### **Test Equipment List**

1. Oscilloscope: DSA91304A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: DSA91304A

Voltage per division: 500mV

Time scale: 5ns

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

1. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 218. Test Condition for SI – Storage mSATA**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |
| --- | --- | --- | --- |
| mSATA Transmit | | | |
| Probing points | Parameters | Specification | |
| Min | Max |
| C1833.1 and C1834.1 | Eye jit RMS (ps) |  | 100 |
| Eye Width (ps) | 166.66 |  |
| Eye Height (mV) | 695.2 |  |
| Data TIE (ps) | -11 | 11 |
| Data Rate (Gb/s) |  | 3 |
| Voltage peak to peak (mV) | 800 |  |
| mSATA Receive | | | |
| Probing points | Parameters | Specification | |
| Min | Max |
| C1835.2 and C1836.2 | Eye jit RMS (ps) |  | 100 |
| Eye Width (ps) | 166.66 |  |
| Eye Height (mV) | 695.2 |  |
| Data TIE (ps) | -11 | 11 |
| Data Rate (Gb/s) |  | 3 |
| Voltage peak to peak (mV) | 800 |  |

**Table 219. Requirements for SI – Storage mSATA**

##### **Test Procedure**

1. Configure DC power supply to give a voltage of 18V.
2. Insert mSATA in GBC board.
3. Probe the mSATA TX signal at C1833.1 and C1834.1 using differential probe.
4. Probe the mSATA RX signal at C1835.2 and C1836.2 using differential probe.
5. Plot eye diagram and analyze the eye characteristics
6. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 8 and 21 of GBC schematic Life-2.

#### Test Case: I/O Stress (Test ID: CPU.11.2)

##### **Description**

1. **Purpose**The purpose of the test case is to validate mSATA memory access when mSATA lines are under stress.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case causes mSATA to hang/ not perform properly under stress. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 220. Impact of Failure of I/O Stress – Storage mSATA**

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

1. OS loaded MSATA
2. FIO utility

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 221. Test Condition for I/O Stress – Storage mSATA**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| I/O Stress | FIO utility | FIO utility will stress the mSATA lines to their maximum performance. While they are under stress, mSATA memory should be accessible with no errors. |

**Table 222. Requirements for I/O Stress – Storage mSATA**

##### **Test Procedure**

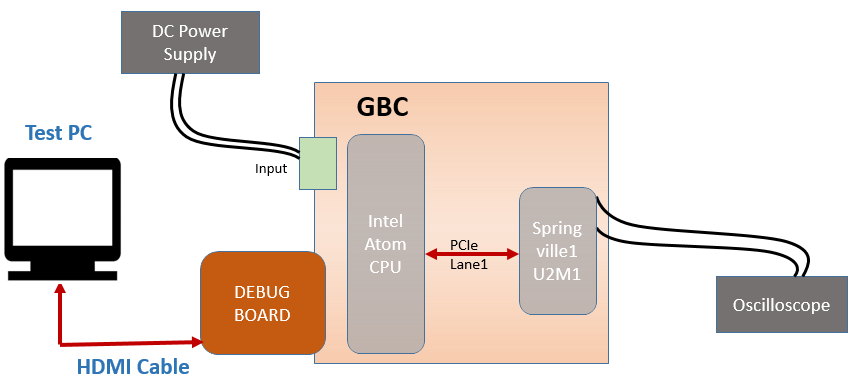
1. Connect Debug board to GBC board.
2. Connect a monitor to debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. Run FIO utility in the Console (SOC).
5. Validate the output as per the above requirement.

##### **Reference**

Further details can be found in Page 8 and 21 of GBC schematic Life-2.

### Springville1 - PCIe

#### Test Setup



**Figure 24. SpringVille1 – PCIe- Test Setup Diagram**

#### Test Case: Springville1 - PCIe (Test ID: CPU.13.1)

##### **Description**

1. **Purpose**

The purpose of this test case is to check and validate the electrical parameters and signal integrity of PCIe interface between Intel processor (U3) and Springville1 (U2M1).

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Communication between springville1 and Intel will fail resulting in data loss |
| Performance | NA |  |
| Compliance | NA |  |

**Table 223. Impact of Failure – Springville1 – PCIe Lane1**

1. **Measurement Locations**
2. Transmitter Lane1:

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| PCIE1\_TXP\_LAN | C2B30.1 |
| PCIE1\_TXN\_LAN | C2B29.1 |

**Table 224. Measurement Locations – Transmitter Springville1 – PCIe Lane1**

1. Receiver Lane1:

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| PCIE1\_RXP\_LAN | C2M4.1 |
| PCIE1\_RXN\_LAN | C2M6.1 |

**Table 225. Measurement Locations – Receiver Springville1 – PCIe Lane1**

##### **Test Equipment List**

1. AUX Power supply unit: Agilent E3634A
2. Oscilloscope: DSA91304A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 20V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. mSATA
3. Debug board
4. Monitor

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal Input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 226. Test Condition – Springville1 – PCIe Lane1**

##### **DUT Settings for Transmitter tests**

Remove Springville1 IC (U2M1). Terminate the Tx lane1 lines from Intel processor by mounting a 50-ohm resistor on pin no 23 and 24 of U2M1. By doing so, PCIe compliance pattern as per section 4.2.8 of PCIe base specification ver. 2.1 is generated.

##### **DUT Settings for Receiver tests**

Mount back Springville1 IC (U2M1). Terminate the Rx lane1 lines from Springville1 (U2M1) by lifting capacitor side C2M4.1 and C2M6.1 and terminating the line by mounting a 50-ohm resistor. By doing so, PCIe compliance pattern as per section 4.2.8 of PCIe base specification ver. 2.1 is generated.

##### **Requirements**

NA

##### **Test Procedure**

* **Transmitter Test:**

1. Probe PCIE1\_TXP\_LAN and PCIE1\_TXN\_LAN at C2B30.1 and C2B29.1 respectively.
2. Run the test utility N5393D in the infiniium oscilloscope. To configure the test suite, select PCIe version as 2.0, Transmitter tests, Device1, Lane1, and speed as 2.5GT/s. In select tests option in utility, select transmitter tests and run all the selected test cases.
3. The test utility generates the test report for all the test cases selected with the pass or fail criteria and its % margin.

* **Receiver Test:**

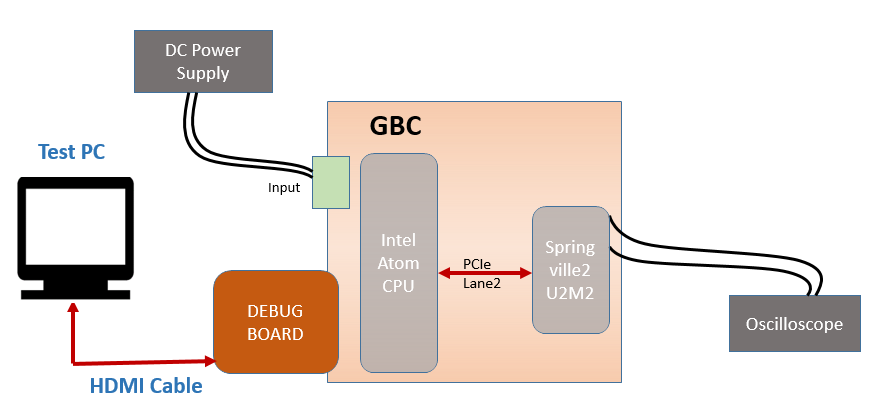
1. Probe PCIE1\_RXP\_LAN and PCIE1\_RXN\_LAN at C2M4.1 and C2M6.1 respectively.
2. Run the test utility N5393D in the infiniium oscilloscope. To configure the test suite, select PCIe version as 2.0, Receiver tests, Device1, Lane1, and speed as 2.5GT/s. In select tests option in utility, select receiver tests and run all the selected test cases.
3. The test utility generates the test report for all the test cases selected with the pass or fail criteria and its % margin.

##### **Reference**

Further details can be found in Page 9 and 23 of GBC schematic Ver. Life-2.

### Springville2 - PCIe

#### Test Setup



**Figure 25. SpringVille2 – PCIe- Test Setup Diagram**

#### Test Case: Springville2 - PCIe (Test ID: CPU.13.2)

##### **Description**

1. **Purpose**

The purpose of this test case is to check and validate the electrical parameters and signal integrity of PCIe interface between Intel processor (U3) and Springville2 (U2M2).

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Communication between springville2 and Intel will fail resulting in data loss |
| Performance | NA |  |
| Compliance | NA |  |

**Table 227. Impact of Failure – Springville2 – PCIe Lane2**

1. **Measurement Locations**
2. Transmitter Lane 2:

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| PCIE2\_TXP\_LAN | C2B32.1 |
| PCIE2\_TXN\_LAN | C2B31.1 |

**Table 228. Measurement Locations – Transmitter Springville2 – PCIe Lane2**

1. Receiver Lane 2:

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| PCIE2\_RXP\_LAN | C2M22.1 |
| PCIE2\_RXN\_LAN | C2M21.1 |

**Table 229. Measurement Locations – Receiver Springville2 – PCIe Lane2**

##### **Test Equipment List**

1. AUX Power supply unit: Agilent E3634A
2. Oscilloscope: DSA91304A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 20V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. mSATA
3. Debug board
4. Monitor

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal Input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 230. Test Condition – Springville2 – PCIe Lane2**

##### **DUT Settings for Transmitter tests**

Remove Springville2 IC (U2M2). Terminate the Tx lane2 lines from Intel processor by mounting a 50-ohm resistor on pin no 23 and 24 of U2M2. By doing so, PCIe compliance pattern as per section 4.2.8 of PCIe base specification ver. 2.1 is generated.

##### **DUT Settings for Receiver tests**

Mount back Springville2 IC (U2M2). Terminate the Rx lane2 lines from Springville2 (U2M2) by lifting capacitor side C2M22.1 and C2M21.1 and terminating the line by mounting a 50-ohm resistor. By doing so, PCIe compliance pattern as per section 4.2.8 of PCIe base specification ver. 2.1 is generated.

##### **Requirements**

NA

##### **Test Procedure**

* **Transmitter Test:**

1. Probe PCIE2\_TXP\_LAN and PCIE2\_TXN\_LAN at C2B32.1 and C2B31.1 respectively.
2. Run the test utility N5393D in the infiniium oscilloscope. To configure the test suite, select PCIe version as 2.0, Transmitter tests, Device1, Lane2, and speed as 2.5GT/s. In select tests option in utility, select transmitter tests and run all the selected test cases.
3. The test utility generates the test report for all the test cases selected with the pass or fail criteria and its % margin.

* **Receiver Test:**

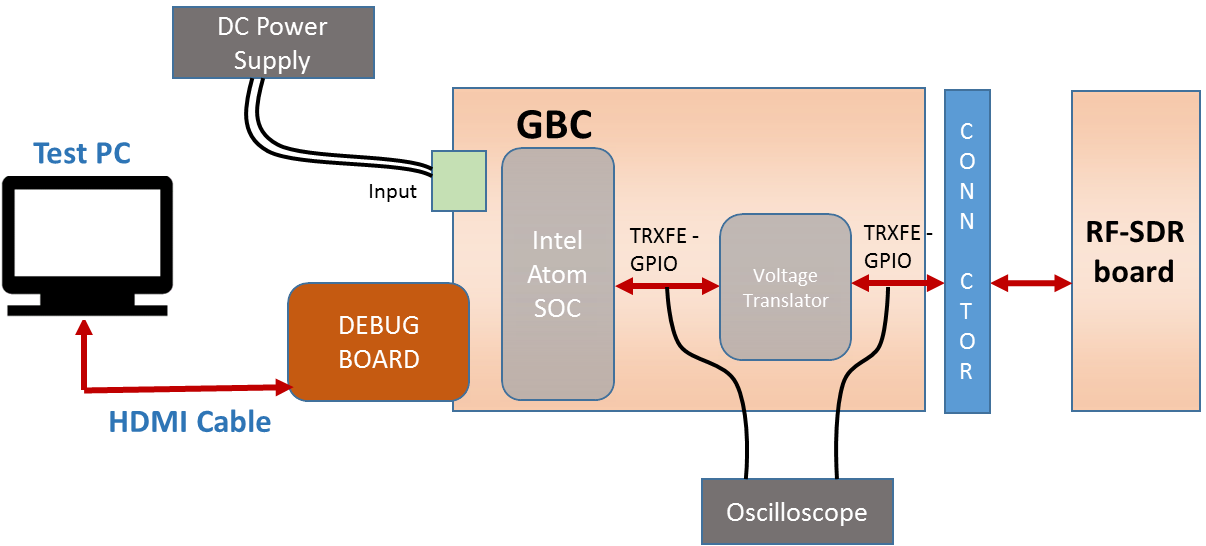
1. Probe PCIE2\_RXP\_LAN and PCIE2\_RXN\_LAN at C2M22.1 and C2M21.1 respectively.
2. Run the test utility N5393D in the infiniium oscilloscope. To configure the test suite, select PCIe version as 2.0, Receiver tests, Device1, Lane2, and speed as 2.5GT/s. In select tests option in utility, select receiver tests and run all the selected test cases.
3. The test utility generates the test report for all the test cases selected with the pass or fail criteria and its % margin.

##### **Reference**

Further details can be found in Page 9 and 24 of GBC schematic Ver. Life-2

### TRXFE - GPIO

#### Test Setup



**Figure 26. TRXFE GPIO - Test Setup Diagram**

#### Test Case: Control outputs functional validation (Test ID: CPU.15.2)

##### **Description**

1. **Purpose**The purpose of the test case is to execute the control outputs functional validation of TRXFE- GPIO signals.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case will cause the GPIO lines to not toggle and hence not work as per design. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 231. Impact of Failure of Control outputs FV – TRXFE GPIO**

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

1. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 232. Test Condition for Control outputs FV – TRXFE GPIO**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| Control outputs functional validation | Toggling of TRXFE - GPIO signals | Toggle the GPIO lines by using GPIO Sysfs Interface in Linux. |

**Table 233. Requirements for Control outputs FV – TRXFE GPIO**

##### **Test Procedure**

1. Connect Debug board to GBC board.
2. Connect a monitor to debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. Open the terminal and run the command to toggle the GPIO lines.
5. Validate the output as per the above requirement.

##### **Reference**

Further details can be found in Page 9, 76 and 84 of GBC schematic Life-2.

#### Test Case: Signal Characteristics (Test ID: CPU.15.3)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the signal characteristics of TRXFE- GPIO signals.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | Failure of this test case will result in improper functioning of the GPIO lines. |
| Compliance | NA |  |

**Table 234. Impact of Failure of SI – TRXFE GPIO**

1. **Measurement Locations**
2. R10546, R10547, R10548 and R10549
3. R10542, R10543, R10528 and R10529

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50ms

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

1. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 235. Test Condition for SI – TRXFE GPIO**

##### **DUT Settings**

Resistor R10540 is removed and Pin 2 of the resistor is connected to ground to enable the level shifter.

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min(V) | Max(V) |
| **Before Level Shifter** | | | | |
| SOC\_TRXFE\_GPIO1 | R10546 | VLOW (V) | 0 | 0.63 |
| VHIGH (V) | 1.17 | 1.8 |
| Positive Over-shoot (V) | 0 | 0.18 |
| Negative Over-shoot (V) | 0 | 0.18 |
| SOC\_TRXFE\_GPIO2 | R10547 | VLOW (V) | 0 | 0.63 |
| VHIGH (V) | 1.17 | 1.8 |
| Positive Over-shoot (V) | 0 | 0.18 |
| Negative Over-shoot (V) | 0 | 0.18 |
| SOC\_TRXFE\_GPIO3 | R10548 | VLOW (V) | 0 | 0.63 |
| VHIGH (V) | 1.17 | 1.8 |
| Positive Over-shoot (V) | 0 | 0.18 |
| Negative Over-shoot (V) | 0 | 0.18 |
| SOC\_TRXFE\_GPIO4 | R10549 | VLOW (V) | 0 | 0.63 |
| VHIGH (V) | 1.17 | 1.8 |
| Positive Over-shoot (V) | 0 | 0.18 |
| Negative Over-shoot (V) | 0 | 0.18 |
| **After Level Shifter** | | | | |
| ISO\_SOC\_TRXFE\_GPIO1 | R10542 | VLOW (V) | -0.3 | 0.8 |
| VHIGH (V) | 2 | 3.6 |
| Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |
| ISO\_SOC\_TRXFE\_GPIO2 | R10543 | VLOW (V) | -0.3 | 0.8 |
| VHIGH (V) | 2 | 3.6 |
| Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |
| ISO\_SOC\_TRXFE\_GPIO3 | R10528 | VLOW (V) | -0.3 | 0.8 |
| VHIGH (V) | 2 | 3.6 |
| Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |
| ISO\_SOC\_TRXFE\_GPIO4 | R10529 | VLOW (V) | -0.3 | 0.8 |
| VHIGH (V) | 2 | 3.6 |
| Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |

**Table 236. Requirements for SI – TRXFE GPIO**

##### **Test Procedure**

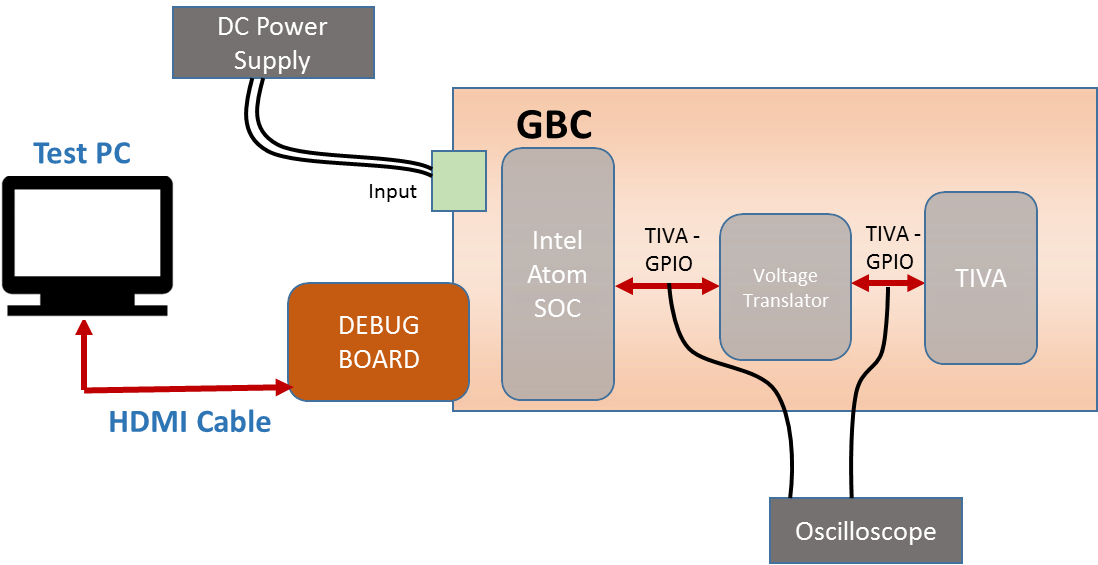
1. Connect Debug board to GBC board.
2. Connect a monitor to debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. Open the terminal and run the command to toggle the GPIO lines.
5. Probe the TRXFE - GPIO lines before level shifter at R10546, R10547, R10548 and R10549 and after level shifter at R10542, R10543, R10528 and R10529 respectively verify the signal characteristics.
6. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

###### **Reference**

Further details can be found in Page 9, 76 and 84 of GBC schematic Life-2.

### TIVA - GPIO

* + - 1. **Test Setup**



**Figure 27. TIVA GPIO - Test Setup Diagram**

* + - 1. **Test Case:Control inputs functional validation *(Test ID: CPU.17.1)*** 
         1. **Description**

1. **Purpose**The purpose of the test case is to execute the control inputs functional validation of TIVA- GPIO signals.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case will cause the GPIO lines to not toggle and hence not work as per design. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 237. Impact of Failure of Control inputs FV – TIVA GPIO**

* + - * 1. **Test Equipment List**

1. DC power supply: E3633A
   * + - 1. **Equipment Settings**
2. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

* + - * 1. **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor
   * + - 1. **Software Requisites**
4. OS loaded MSATA
   * + - 1. **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 238. Test Condition for Control inputs FV – TIVA GPIO**

* + - * 1. **DUT Settings**

NA

* + - * 1. **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| Control inputs functional validation | Toggling of TIVA - GPIO signals | Toggle the GPIO lines by using GPIO Sysfs Interface in Linux. |

**Table 239. Requirements for Control inputs FV – TIVA GPIO**

* + - * 1. **Test Procedure**

1. Connect Debug board to GBC board.
2. Connect a monitor to debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. Open the terminal and run the command to toggle the GPIO lines.
5. Validate the output as per the above requirement.
   * + - 1. **Reference**

Further details can be found in Page 12, 60 and 83 of GBC schematic Life-2.

* + - 1. **Test Case:Control outputs functional validation *(Test ID: CPU.17.2)*** 
         1. **Description**

1. **Purpose**The purpose of the test case is to execute the control outputs functional validation of TIVA- GPIO signals.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case will cause the GPIO lines to not toggle and hence not work as per design. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 240. Impact of Failure of Control outputs FV – TIVA GPIO**

* + - * 1. **Test Equipment List**

1. DC power supply: E3633A
   * + - 1. **Equipment Settings**
2. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

* + - * 1. **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor
   * + - 1. **Software Requisites**
4. MSATA with OS loaded
   * + - 1. **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 241. Test Condition for Control outputs FV – TIVA GPIO**

* + - * 1. **DUT Settings**

NA

* + - * 1. **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| Control outputs functional validation | Toggling of TIVA - GPIO signals | Toggle the GPIO lines by using GPIO Sysfs Interface in Linux. |

**Table 242. Requirements for Control outputs FV – TIVA GPIO**

* + - * 1. **Test Procedure**

1. Connect Debug board to GBC board.
2. Connect a monitor to debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. Open the terminal and run the command to toggle the GPIO lines.
5. Validate the output as per the above requirement.
   * + - 1. **Reference**

Further details can be found in Page 12, 60 and 83 of GBC schematic Life-2.

* + - 1. **Test Case:Signal Characteristics *(Test ID: CPU.17.3)*** 
         1. **Description**

1. **Purpose**The purpose of the test case is to execute the control outputs functional validation of TIVA- GPIO signals.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | Failure of this test case will result in improper functioning of the GPIO lines. |
| Compliance | NA |  |

**Table 243. Impact of Failure of SI – TIVA GPIO**

1. **Measurement Locations**

R10514, R10516

* + - * 1. **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A
   * + - 1. **Equipment Settings**
3. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 1s

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

* + - * 1. **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor
   * + - 1. **Software Requisites**
4. OS loaded MSATA
   * + - 1. **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 244. Test Condition for SI – TIVA GPIO**

##### **DUT Settings**

Resistor R10511 is removed and Pin 2 of the resistor is connected to ground to enable the level shifter.

* + - * 1. **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min(V) | Max(V) |
| **Before Level Shifter** | | | | |
| ISO\_TIVA\_SOC\_GPIO2 | R10514 | VLOW (V) | 0 | 0.63 |
| VHIGH (V) | 1.17 | 1.8 |
| Positive Over-shoot (V) | 0.00 | 0.18 |
| Negative Over-shoot (V) | 0.00 | 0.18 |
| **After Level Shifter** | | | | |
| TIVA\_SOC\_GPIO2 | R10516 | VLOW (V) | 0.00 | 1.16 |
| VHIGH (V) | 2.15 | 4.00 |
| Positive Over-shoot (V) | 0.00 | 0.33 |
| Negative Over-shoot (V) | 0.00 | 0.33 |

**Table 245. Requirements for SI – TIVA GPIO**

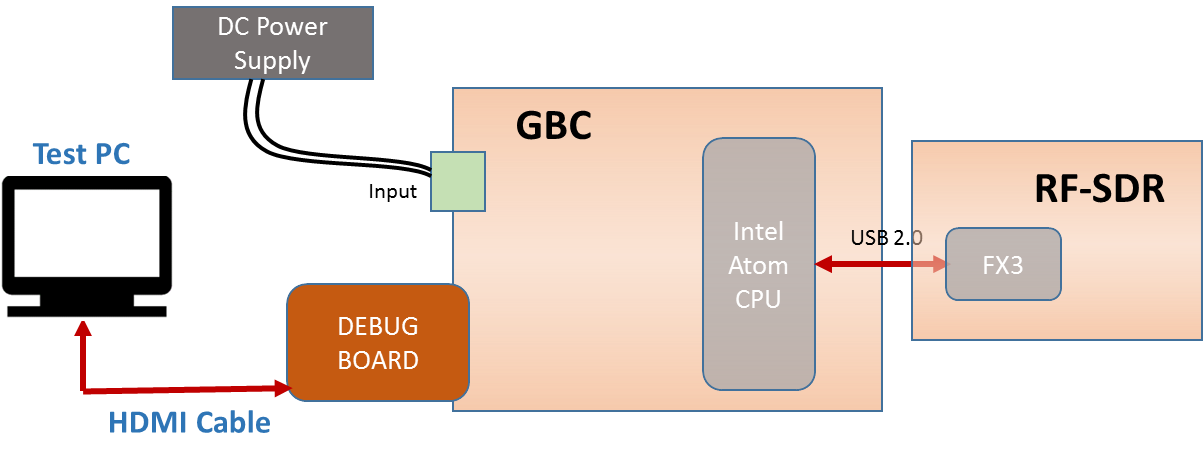
* + - * 1. **Test Procedure**

1. Connect Debug board to GBC board.
2. Connect a monitor to debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. Open the terminal and run the command to toggle the GPIO lines.
5. Probe the GPIO2 signal at R10514 before level shifter and at R10516 after level shifter and verify the signal characteristics.
6. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.
   * + - 1. **Reference**

Further details can be found in Page 12, 60 and 83 of GBC schematic Life-2.

### TRXFE – FX3 – USB2.0

#### Test Setup

******

**Figure 28. TRXFE FX3 USB2.0 - Test Setup Diagram**

#### Test Case: Electrical Validation (Test ID: CPU.19.1)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the electrical characteristics of USB2.0 interface between GBC and RF-SDR.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | Failure of this test case results in communication failure between GBC and RF-SDR through USB2.0 |
| Compliance | NA |  |

**Table 246. Impact of Failure of EV – TRXFE FX3 USB2.0**

1. **Measurement Locations**

R206.2, R208.2

##### **Test Equipment List**

1. Oscilloscope: DSA91304A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: DSA91304A

Voltage per division: 1V

Time scale: 50µs

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. RF-SDR board
3. Debug board
4. Monitor

##### **Software Requisites**

1. OS (Linux 14.4.4) loaded MSATA with Uhd drivers in it
2. Core Boot without USB
3. Dediprog engineering

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 247. Test Condition for EV – TRXFE FX3 USB2.0**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| USB 2.0 | Electrical characteristics | All the measuring parameters should pass |

##### **Test Procedure**

1. Flash “without USB core boot” on SPI NOR Flash using SF-100.
2. Connect Debug board to GBC board.
3. Connect a monitor to Debug board.
4. Configure DC power supply to give a voltage of 18V.
5. Give “sudo uhd\_usrp\_probe” command in the terminal.
6. Make sure communication is happening between GBC and RF-SDR is through USB 2.0.
7. Capture one frame of data (USB 2.0 signals) by probing at R206 (USB\_DP0) and R208 (USB\_DN0) and save as .csv format.
8. Input this .csv file to “USBET20” tool provided by USB.org, an official analysis tool for certifying signal quality and inrush current published by the USB-IF.  Please be sure to run captured signal quality and inrush current test data through this tool for an official assessment of the measurement.
9. Link to download USBET20 tool is - <http://www.usb.org/developers/tools/usb20_tools/>
10. This will generate a report in .html format.
11. Make sure all the measuring parameters are pass.

##### **Reference**

Further details can be found in Page 12 and 76 GBC schematic Ver. Life-2 and page 19,18 and 15 of Debug board schematic Life-2.

#### Test Case: Throughput measurement (Test ID: CPU.19.2)

##### **Description**

1. **Purpose**The purpose of the test case is to validate USB 2.0 throughput.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | System requirement will not be met in case of failure of this test case. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 248. Impact of Failure of Throughput measurement** **– USB 2.0**

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

OS loaded MSATA with cyusb\_linux application

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 249. Test Condition for Throughput measurement – USB 2.0**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| Memory DDR | Throughput | 25 MB/s |

**Table 250. Requirements for Throughput measurement – USB 2.0**

##### **Test Procedure**

1. Connect Debug board to GBC board.
2. Connect a monitor to debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. Install the FX3 Utility, by running the installation script. (./install.sh).
5. Run the cyusb\_linux application.
6. Select the device from the list, and under the program tab download the USBIso image, .img file with burst 8 and mult 3.
7. Under the Descriptors tab, select the device from the list of devices.
8. Under the Data Transfers tab, start the process to know the throughput achieved.

##### **Reference**

Further details can be found in Page 12 and 76 GBC schematic Ver. Life-2

#### Test Case: Functional Validation (Test ID: CPU.19.3)

##### **Description**

1. **Purpose**The purpose of the test case is to validate USB 2.0 interface between GBC and RF-SDR board.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case results in communication failure between GBC and RF-SDR through USB2.0 |
| Performance | NA |  |
| Compliance | NA |  |

**Table 251. Impact of Failure of TRXFE – FX3 – USB2.0**

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. RF-SDR board
4. Monitor

##### **Software Requisites**

1. OS (Linux 14.4.4) loaded MSATA with Uhd drivers in it
2. CoreBoot without USB
3. Dediprog engineering

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 252. Test Condition for FV – TRXFE – FX3 – USB2.0**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Result** |  |
| USB 2.0 Interface | Communication should happen through USB 2.0 when “sudo uhd\_usrp\_probe” command is given. | |

**Table 253. Requirements for FV – TRXFE – FX3 – USB2.0**

##### **Test Procedure**

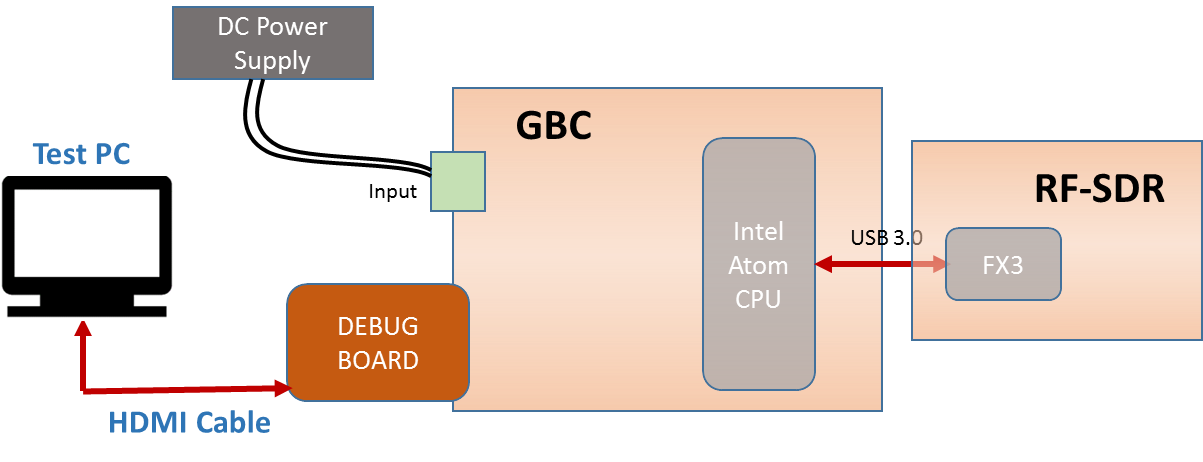
1. Flash “without USB core boot” on SPI NOR Flash using SF-100.
2. Connect Debug board to GBC board.
3. Connect a Test PC to Debug board.
4. Configure DC power supply to give a voltage of 18V.
5. Give “sudo uhd\_usrp\_probe” command in the terminal.
6. Make sure communication is happening between GBC and RF-SDR is through USB 2.0.

##### **Reference**

Further details can be found in Page 12 and 76 GBC schematic Ver. Life-2 and page 19,18 and 15 of Debug board schematic Life-2.

### TRXFE – FX3 – USB3.0

#### Test Setup



**Figure 29. TRXFE – FX3 – USB3.0 - Test Setup Diagram**

#### Test Case Throughput measurement (Test ID: CPU.20.2)

##### **Description**

1. **Purpose**The purpose of the test case is to validate USB 3.0 throughput.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | System requirement will not be met in case of failure of this test case. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 254. Impact of Failure of Throughput measurement** **– USB 3.0**

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

OS loaded MSATA with cyusb\_linux application

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 255. Test Condition for Throughput measurement – USB 3.0**

##### **DUT Settings**

Remove the following capacitors and short the path because more number of decoupling capacitors are present in the path:

C1979, C1980, C1984, C1985, C1988 and C1989

Remove the following resistors:

R10627, R10628, R10629 and R10630.

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| Memory DDR | Throughput | 240 MB/s |

**Table 256. Requirements for Throughput measurement – USB 3.0**

**NOTE:** Expected throughput is 240 MB/s as per image provided by Cypress.

##### **Test Procedure**

1. Connect Debug board to GBC board.
2. Connect a monitor to debug board using HDMI cable.
3. Configure DC power supply to give a voltage of 18V.
4. Install the FX3 Utility, by running the installation script. (./install.sh).
5. Run the cyusb\_linux application.
6. Select the device from the list, and under the program tab download the USBIso image, .img file with burst 8 and mult 3.
7. Under the Descriptors tab, select the device from the list of devices.
8. Under the Data Transfers tab, start the process to know the throughput achieved.

##### **Reference**

Further details can be found in Page 12, 85 and 76 GBC schematic Ver. Life-2.

#### Test Case: Functional Validation (Test ID: CPU.20.3)

##### **Description**

1. **Purpose**The purpose of the test case is to validate USB 3.0 interface between GBC and RF-SDR board.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case results in communication failure between GBC and RF-SDR through USB3.0 |
| Performance | NA |  |
| Compliance | NA |  |

**Table 257. Impact of Failure of TRXFE – FX3 – USB3.0**

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. RF-SDR board
4. Monitor

##### **Software Requisites**

1. OS (Linux 14.4.4) loaded MSATA with Uhd drivers
2. CoreBoot with USB
3. Dediprog engineering

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 258. Test Condition for FV – TRXFE – FX3 – USB3.0**

##### **DUT Settings**

Remove the following capacitors and short the path because more number of decoupling capacitors are present in the path:

C1979, C1980, C1984, C1985, C1988 and C1989

Remove the following resistors:

R10627, R10628, R10629 and R10630.

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Result** |  |
| USB 3.0 Interface | Communication should happen through USB 3.0 when “sudo uhd\_usrp\_probe” command is given. | |

**Table 259. Requirements for FV – TRXFE – FX3 – USB3.0**

##### **Test Procedure**

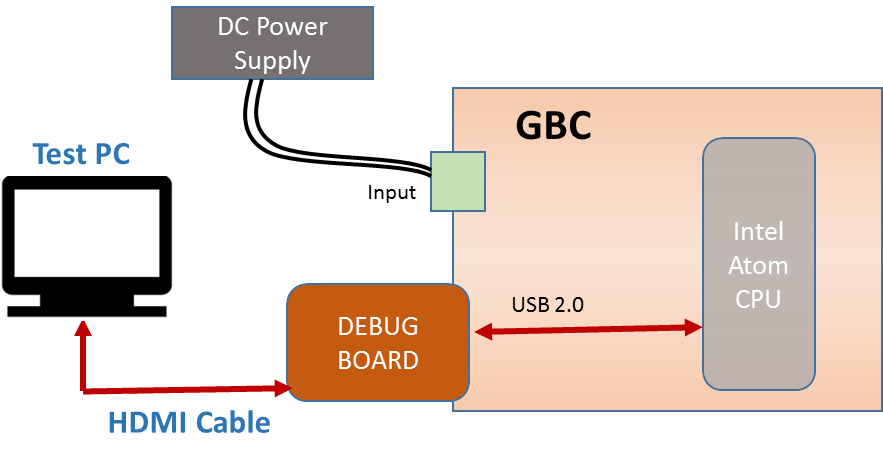
1. Flash “with usb core boot” on SPI NOR Flash using SF-100 to configure FX3.
2. Connect Debug board to GBC board.
3. Connect a Test PC to debug board.
4. Configure DC power supply to give a voltage of 18V.
5. Give “sudo uhd\_usrp\_probe” command in the terminal.
6. Make sure communication is happening between GBC and RF-SDR is through USB 3.0.

##### **Reference**

Further details can be found in Page 12, 85 and 76 GBC schematic Ver. Life-2 and page 17, 19 and 15 of Debug board schematic Life-2.

### Debug USB2.0

#### Test Setup



**Figure 30. Debug USB2.0 - Test Setup Diagram**

#### Test Case: Functional Validation (Test ID: CPU.21.1)

##### **Description**

1. **Purpose**The purpose of the test case is to validate USB 2.0 in debug board.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case results in communication failure between GBC and USB2.0 device connected to debug board. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 260. Impact of Failure of Debug USB2.0**

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

1. OS loaded MSATA
2. CoreBoot without USB
3. Dediprog engineering

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 261. Test Condition for FV – Debug USB2.0**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| USB 2.0 Interface | Device ID | The USB2.0 device connected to USB 2.0 port in debug board should list under Bus1 when “lsusb –t” command is given. |

**Table 262. Requirements for FV – Debug USB2.0**

##### **Test Procedure**

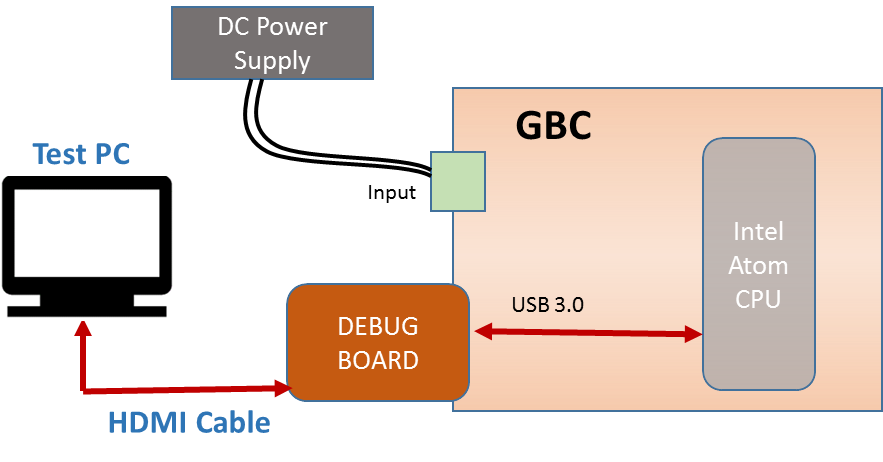
1. Flash “without USB core boot” on SPI NOR Flash using SF-100.
2. Connect Debug board to GBC board.
3. Connect a Test PC to debug board.
4. Configure DC power supply to give a voltage of 18V.
5. A USB2.0 device(pen drive) is connected to USB2.0 port in debug board.
6. Give “lsusb –t” command.
7. This will list out all the devices connected through USB.
8. Make sure that the USB2.0 device should list under Bus1.

##### **Reference**

Further details can be found in Page 12 and 69 of GBC schematic Ver. Life-2 and page 3, 4 and 6 of debug board schematic Life-2.

### Debug USB3.0

#### Test Setup



**Figure 31. Debug USB3.0 - Test Setup Diagram**

#### Test Case: Functional Validation (Test ID: CPU.22.1)

##### **Description**

1. **Purpose**The purpose of the test case is to validate USB 3.0 in debug board.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case results in communication failure between GBC and USB3.0 device connected to debug board. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 263. Impact of Failure of Debug USB3.0**

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor

##### **Software Requisites**

1. OS loaded MSATA with Uhd drivers
2. CoreBoot with USB
3. Dediprog engineering

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 264. Test Condition for FV – Debug USB3.0**

##### **DUT Settings**

Remove the following capacitors and short the path because more number of decoupling capacitors are present in the path:

C1979, C1980, C1986 and C1987.

Remove the following resistors:

R10627, R10628, R10629 and R10630.

In debug board, remove C4P4 and C4P3 and short the path.

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| USB 3.0 Interface | Device ID | The USB 3.0 device connected to usb 3.0 port in debug board should list under Bus2 when “lsusb –t” command is given. |

**Table 265. Requirements for FV – Debug USB3.0**

##### **Test Procedure**

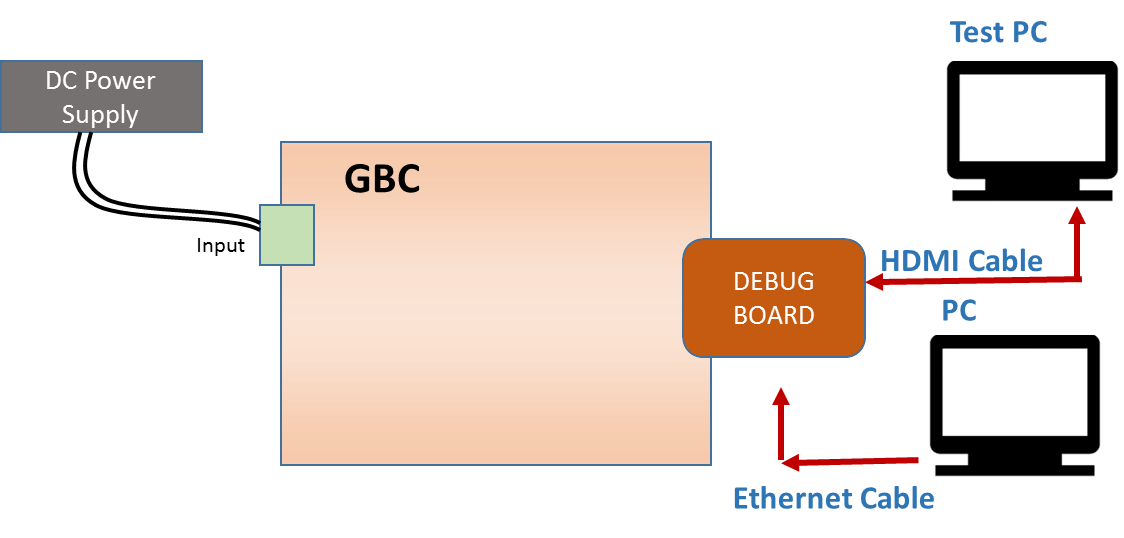
1. Flash with “usb core boot” on SPI NOR Flash using SF-100 to configure FX3.
2. Connect Debug board to GBC board.
3. Connect a Monitor to Debug board.
4. Configure DC power supply to give a voltage of 18V.
5. A USB3.0 pen drive/HDD is connected to USB3.0 port in debug board.
6. The USB3.0 signals at USB switch (U48) is routed to debug connector by toggling operation mode select pin of Mux/Demux switch (U48) using GPIO Sysfs Interface in Linux.
7. Give “lsusb –t” command.
8. This will list out all the devices connected through USB.
9. Make sure that USB3.0 device connected to USB 3.0 port should list under Bus2.

##### **Reference**

Further details can be found in Page 12, 85 and 69 GBC schematic Ver. Life-2 and page 6 and 16 of Debug board schematic Life-2.

### Debug Ethernet

#### Test Setup



**Figure 32. Debug Ethernet - Test Setup Diagram**

#### Test Case: Functional Validation (Test ID: CPU.23.1)

##### **Description**

1. **Purpose**The purpose of the test case is to validate Ethernet port in debug board.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case results in communication failure between GBC System and the system which is connected to Ethernet port of debug board. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 266. Impact of Failure of Debug Ethernet**

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Monitor
4. Linux PC

##### **Software Requisites**

1. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 267. Test Condition for FV – Debug Ethernet**

##### **DUT Settings**

Make U238 selection pin high mount R10661 and unmount R10662.

##### **Requirements**

|  |  |
| --- | --- |
| **Test** | **Result** |
| Debug Ethernet port | The connection should establish between GBC system and the PC connected to debug Ethernet switch. |

**Table 268. Requirements for FV – Debug Ethernet**

##### **Test Procedure**

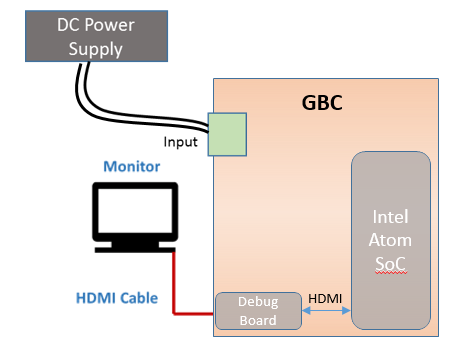
1. Connect Debug board to GBC board.
2. Connect a Monitor to Debug board.
3. Connect a PC to debug Ethernet port.
4. Configure DC power supply to give a voltage of 18V.
5. Establish the connection between GBC system and the external PC using “ping” command.
6. Make sure the communication is established.

##### **Reference**

Further details can be found in Page 86, 87, 26 and 25 of GBC schematic Ver. Life-2 and page 14 and 15 of Debug board schematic Life-2.

### Display - HDMI

#### Test Setup



**Figure 33. Display HDMI - Test Setup Diagram**

* + - 1. **Test Case:Functional Validation *(Test ID: CPU.24.1)*** 
         1. **Description**

1. **Purpose**The purpose of the test case is to validate HDMI interface in debug board.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case will cause the display not to come up which will affect user interaction with the system |
| Performance | NA |  |
| Compliance | NA |  |

**Table 269. Impact of Failure of FV – Display HDMI**

* + - * 1. **Test Equipment List**

1. DC power supply: E3633A
   * + - 1. **Equipment Settings**
2. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

* + - * 1. **Hardware Requisites**

1. GBC board
2. Debug board
   * + - 1. **Software Requisites**
3. Test PC
4. OS loaded MSATA
   * + - 1. **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 270. Test Condition for FV – Display HDMI**

* + - * 1. **DUT Settings**

NA

* + - * 1. **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| HDMI Interface | Display | User can interact with the DUT for all sorts of functions |

**Table 271. Requirements for FV – Display HDMI**

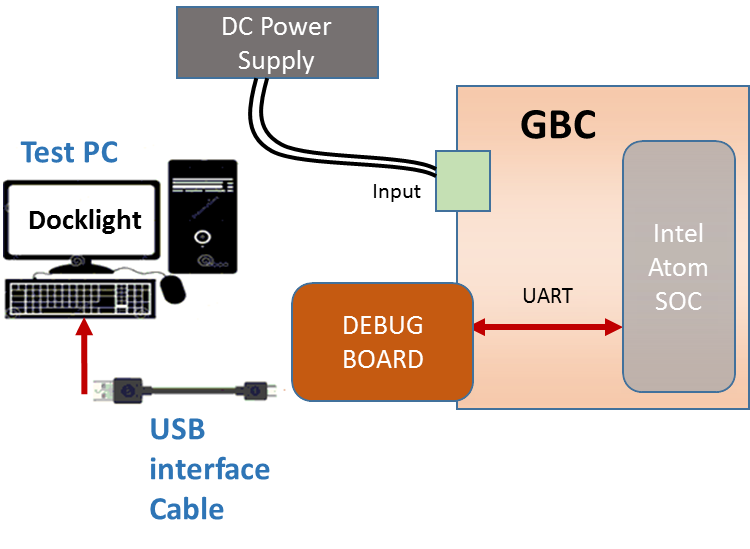
* + - * 1. **Test Procedure**

1. Connect Debug board to GBC board.
2. Connect a PC to the HDMI port (J4N1) of debug board.
3. Configure DC power supply to give a voltage of 18V.
4. If required power rail and HDMI interface are operational, display is seen on the monitor
   * + - 1. **Reference**

Further details can be found in Page 7 and 69 of GBC schematic Life-2 and Page 2 of Debug Schematic Life-2.

### Debug - UART

#### Test Setup



**Figure 34. Debug UART - Test Setup Diagram**

* + - 1. **Test Case:Functional Validation *(Test ID: CPU.25.1)*** 
         1. **Description**

1. **Purpose**The purpose of the test case is to validate UART interface in debug board.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case will cause the GPIO lines to not toggle and hence not work as per design. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 272. Impact of Failure of FV – Debug UART**

* + - * 1. **Test Equipment List**

1. DC power supply: E3633A
   * + - 1. **Equipment Settings**
2. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

* + - * 1. **Hardware Requisites**

1. GBC board
2. Debug board
   * + - 1. **Software Requisites**
3. Test PC with Docklight software
4. OS loaded MSATA
   * + - 1. **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 273. Test Condition for FV – Debug UART**

* + - * 1. **DUT Settings**

Debug board:

1. Bypass U2L1.
2. Remove R64 and R76, R88 and R91
3. Connect R88.1 to R76.2
4. Connect R91.1 to R64.2
   * + - 1. **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| UART Interface | Boot Log | The Intel Atom processor sends boot log through the USB port to the PC during board power up. The data sent can be verified in the application software. |

**Table 274. Requirements for FV – Debug UART**

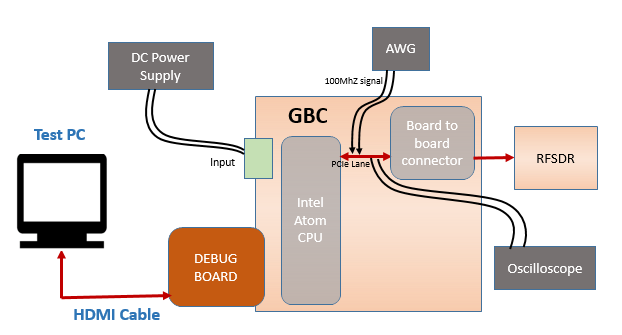
* + - * 1. **Test Procedure**

1. Connect Debug board to GBC board.
2. Connect a PC (with Docklight software) to the USB port (J1N4) of debug board.
3. The Docklight software will be running in the PC.
4. Configure DC power supply to give a voltage of 18V.
5. The Intel Atom processor sends boot log through the USB port to the PC during board power up.
6. The data sent can be verified in the application software.
   * + - 1. **Reference**

Further details can be found in Page 12 and 69 of GBC schematic Life-2 and Page 5, 6 and 10 of Debug Schematic Life-2

### RFSDR – PCIe

#### Test Setup



**Figure 35. RFSDR – PCIe- Test Setup Diagram**

#### Test Case: RFSDR - PCIe (Test ID: CPU.26.1)

##### **Description**

1. **Purpose**

The purpose of this test case is to check and validate the electrical parameters and signal integrity of PCIe interface at 5GT/s between Intel processor (U3) and RFSDR board.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Communication between RFSDR and Intel will fail resulting in data loss |
| Performance | NA |  |
| Compliance | NA |  |

**Table 275. Impact of Failure – Transmitter RFSDR – PCIe Lane0**

1. **Measurement Location**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| PCIE0\_TXP | C2000.1 |
| PCIE0\_TXN | C1999.1 |

**Table 276. Measurement Locations – Transmitter RFSDR – PCIe Lane0**

##### **Test Equipment List**

1. AUX Power supply unit: Agilent E3634A
2. Oscilloscope: DSA91304A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 20V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. mSATA
3. Debug board
4. Monitor

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal Input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 277. Test Condition – Transmitter RFSDR – PCIe Lane0**

##### **DUT Settings for Transmitter tests**

1. Terminate PCIe transmitter lane 0 lines with a 50-ohm resistor. By doing so, PCIe compliance pattern as per section 4.2.8 of PCIe base specification ver. 2.1 is generated.
2. From AWG (arbitrary waveform generator), generate bursts a 100MHz signal for 1ms duration. Connect the output of AWG to PCIE0\_RXP. This ensures the PCIe Tx lines to be transmitting data at 5GT/s speed.

##### **Requirements**

NA

##### **Test Procedure**

* **Transmitter Test:**

1. Probe PCIE0\_TXP PCIE0\_TXN at C2000.1 and C1999.1 respectively.
2. Run the test utility N5393D in the infiniium oscilloscope. To configure the test suite, select PCIe version as 2.0, Transmitter tests, Device1, Lan0, and speed as 5GT/s. In select tests option in utility, select transmitter tests and run all the selected test cases. The test utility generates the test report for all the test cases selected with the pass or fail criteria and its % margin.
3. The test utility generates the test report for all the test cases selected with the pass or fail criteria and its % margin.

##### **Reference**

Further details can be found in Page 9 and 76 of GBC schematic Ver. Life-2.

# TIVA

## Test Purpose and Description

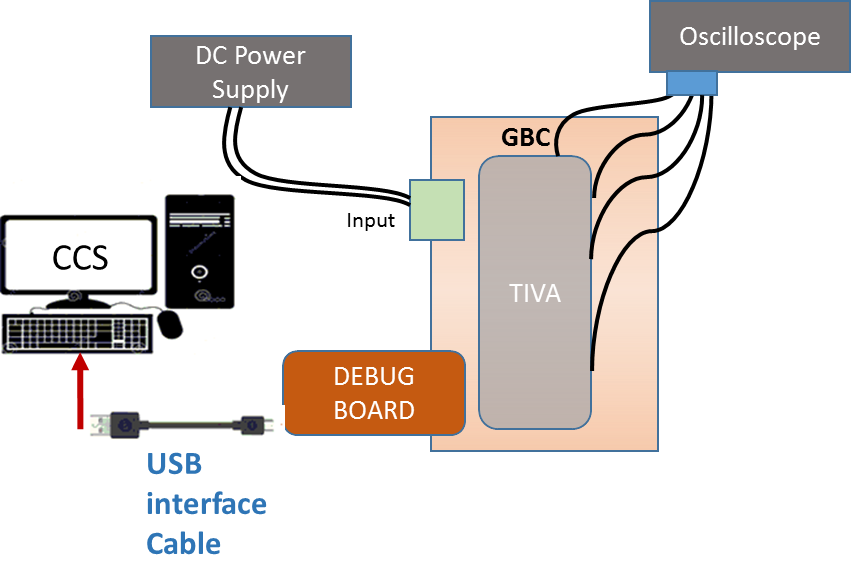
The purpose of TIVA microcontroller is to perform housekeeping operations whose main function will be to control and monitor all power rails, battery charging tasks and various control / configuration / diagnostic tasks (for ex. Configuration of TRX front end etc.).

## TIVA Sub-system constitutes of below components

1. TIVA – Configuration / System reset sequence
2. PSE - I2C
3. Power Monitor - I2C
4. RF SDR IO Exp- I2C
5. Temp Sensor - I2C
6. Sync board - I2C
7. LED board - I2C
8. TIVA GPIO - Control inputs functional validation
9. TIVA GPIO - Control outputs functional validation

### TIVA

#### Test Setup



**NOTE:**

1. Oscilloscope not required for Tiva Configuration.

**Figure 36. TIVA - Test Setup Diagram**

#### Test Case: TIVA Configuration (Test ID: TIV.1.1)

##### **Description**

1. **Purpose**The purpose of this test case is to access TIVA through JTAG and configuring with the help of CCS debug software.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case will result in abnormal functionality of the system. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 278. Impact of Failure of TIVA Configuration**

1. **Measurement Locations**

NA

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board

##### **Software Requisites**

1. Code Composer Studio Tool
2. TIVA Configuration code

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 279. Test Condition for *TIVA Configuration***

##### **DUT Settings**

NA

##### **Requirements**

TIVA Configuration Code

##### **Test Procedure**

1. Connect Debug board to GBC board to flash the code.
2. Connect a Test PC with CCS to debug board.
3. Import the code in Code Composer Studio and configure the debugger.
4. Run the code in CCS
5. Configure DC power supply to give a voltage of 18V.
6. Ensure successfully accessing and programming TIVA controller
7. Make sure the behaviour of TIVA controller as desired.

##### **Reference**

Further details can be found in Page 60 and 74 of GBC schematic Life-2 and Page 8 of Debug Schematic Life-2

#### Test Case: System Reset sequence (Test ID: TIV.1.2)

##### **Description**

1. **Purpose**The purpose of the test case is to validate TIVA system reset sequence.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case will result in abnormal functionality of the system. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 280. Impact of Failure of System Reset sequence**

1. **Measurement Locations**

R10523, R10438, R10165, R10519

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Logic Analyzer Threshold setting: 2V

Time scale: 50ms

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board

##### **Software Requisites**

1. Code Composer Studio Tool
2. System ResetSequence code

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 281. Test Condition for System Reset sequence**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Sl. No** | **Expected sequence** | **Measurement Points** |
| 1 | TIVA\_RESET\_TO\_PROC | R10523 |
| 2 | TIVA\_ETHSW\_RESET | R10438 |
| 3 | TIVA\_TRXFE\_RESET | R10165 |
| 4 | TIVA\_SYNC\_RESET | R10519 |

**Table 282. Requirements for System Reset sequence**

##### **Test Procedure**

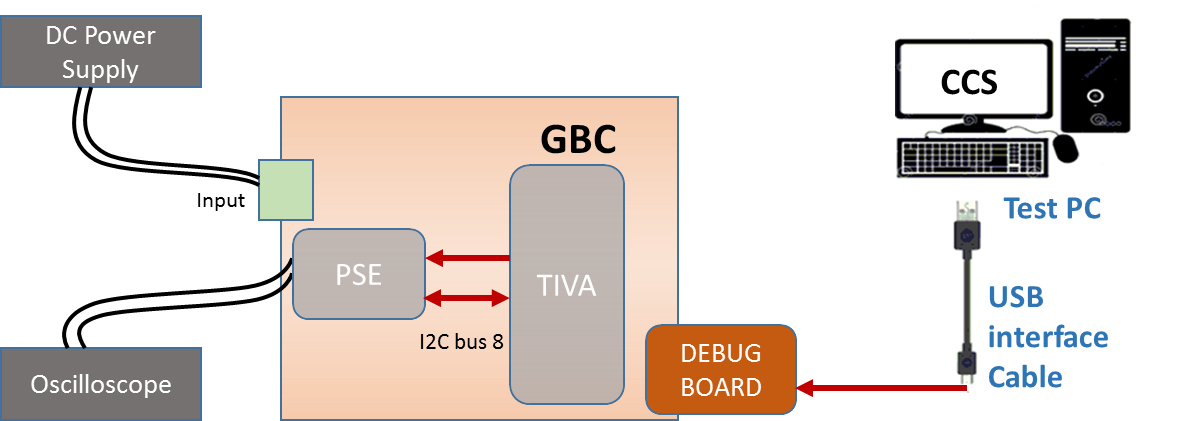
1. Connect Debug board to GBC board to flash the code.
2. Connect a Test PC with CCS to debug board.
3. Import the code in Code Composer Studio.
4. Run the code in CCS.
5. Configure DC power supply to give a voltage of 18V.
6. Set the Logic Analyzer in oscilloscope as mentioned above in Equipment Settings.
7. Probe the reset signals at R10523, R10438, R10165 and R10519 to measure the system reset sequence.
8. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 60, 68 and 80 of GBC schematic Life-2.

### PSE – I2C (LTC4274AIUHF)

#### Test Setup



**Figure 37. PSE I2C -- Test Setup Diagram**

#### Test Case: Electrical Validation (Test ID: TIV.2.1)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the electrical characteristics of I2C interface of PSE controller.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | Failure of this test case will result in improper data from PSE controller. |
| Compliance | NA |  |

**Table 283. Impact of Failure of EV – PSE I2C**

1. **Measurement Locations**

U206.3/ U206.2, U206.6/ U206.7

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. LTPoE++ PSE injector - PS-201G++

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50µs

1. LTPoE++ PSE injector - PS-201G++

Supply Voltage: 53.75 to 56V

Current Limit: 1.6A

##### **Hardware Requisites**

1. GBC board
2. Debug board

##### **Software Requisites**

1. Code Composer Studio Tool
2. Tiva-PSE I2C code

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 284. Test Condition for EV– PSE I2C**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| **Before Isolator** | | | | |
| TIVA\_PSE\_I2C8\_SCLK | U206.3 | VLOW (max) (V) | 0 | 0.5 |
| VHIGH (min) (V) | 2.31 | 3.3 |
| Rise time (ns) | 0 | 1000 |
| Fall time (ns) | 0 | 300 |
| Frequency (kHz) | 0 | 100 |
| TIVA\_PSE\_I2C8\_SDA | U206.2 | VLOW (max) (V) | 0 | 0.5 |
| VHIGH (min) (V) | 2.31 | 3.3 |
| Rise time (ns) | 0 | 1000 |
| Fall time (ns) | 0 | 300 |
| **After Isolator** | | | | |
| PSE\_I2CSCL | U206.6 | VLOW (max) (V) | -0.5 | 0.8 |
| VHIGH (min) (V) | 2.2 | 3.8 |
| Rise time (ns) | 0 | 1000 |
| Fall time (ns) | 0 | 300 |
| Frequency (kHz) | 0 | 100 |
| PSE\_I2CSDA | U206.7 | VLOW (max) (V) | -0.5 | 0.8 |
| VHIGH (min) (V) | 2.2 | 3.8 |
| Rise time (ns) | 0 | 1000 |
| Fall time (ns) | 0 | 300 |

**Table 285. Requirements for EV– PSE I2C**

##### **Test Procedure**

1. Connect Debug board to GBC board to flash the code.
2. Connect a Test PC with CCS to debug board.
3. Import the code in Code Composer Studio.
4. Configure DC power supply to give a voltage of 18V.
5. Probe the I2C signal at U206.3 (SCL), U206.2 (SDA) for before isolator and U206.6 (SCL), U206.7 (SDA) for after isolator.
6. Run the code in CCS.
7. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 45 and 46 of GBC schematic Life-2.

#### Test Case: Signal Integrity (Test ID: TIV.2.2)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the signal integrity of PSE controller.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | Failure of this test case will result in improper data from PSE controller. |
| Compliance | NA |  |

**Table 286. Impact of Failure of SI – PSE I2C**

1. **Measurement Locations**

U206.3/ U206.2, U206.6/ U206.7

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. LTPoE++ PSE injector - PS-201G++

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50µs

1. LTPoE++ PSE injector - PS-201G++

Supply Voltage: 53.75 to 56V

Current Limit: 1.6A

##### **Hardware Requisites**

1. GBC board
2. Debug board

##### **Software Requisites**

1. Code Composer Studio Tool
2. Tiva-PSE I2C code

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 287. Test Condition for SI – PSE I2C**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| **Before Isolator** | | | | |
| TIVA\_PSE\_I2C8\_SCLK | U206.3 | Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |
| TIVA\_PSE\_I2C8\_SDA | U206.2 | data set-up time (ns) | 240 | 10000 |
| data hold time (ns) | 240 | 10000 |
| Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |
| **After Isolator** | | | | |
| PSE\_I2CSCL | U206.6 | Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |
| PSE\_I2CSDA | U206.7 | data set-up time (ns) | 240 | 10000 |
| data hold time (ns) | 240 | 10000 |
| Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |

**Table 288. Requirements for SI – PSE I2C**

##### **Test Procedure**

1. Connect Debug board to GBC board to flash the code.
2. Connect a Test PC with CCS to debug board.
3. Import the code in Code Composer Studio.
4. Configure DC power supply to give a voltage of 18V.
5. Probe the I2C signal at U206.3 (SCL), U206.2 (SDA) for before isolator and U206.6 (SCL), U206.7 (SDA) for after isolator.
6. Run the code in CCS.
7. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 45 and 46 of GBC schematic Life-2.

#### Test Case: Functional Validation (Test ID: TIV.2.3)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the I2C interface of PSE controller.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Registers of PSE controller become inaccessible on failure of this test case. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 289. Impact of Failure of FV – PSE I2C**

##### **Test Equipment List**

1. LTPoE++ PSE injector - PS-201G++

##### **Equipment Settings**

1. LTPoE++ PSE injector - PS-201G++

Supply Voltage: 53.75 to 56V

Current Limit: 1.6A

##### **Hardware Requisites**

1. GBC board
2. Debug board

##### **Software Requisites**

1. Code Composer Studio Tool
2. Tiva-PSE I2C code

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 290. Test Condition for FV – PSE I2C**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| I2C Interface | Device ID | Read Device ID, 70 |

**Table 291. Requirements for FV – PSE I2C**

##### **Test Procedure**

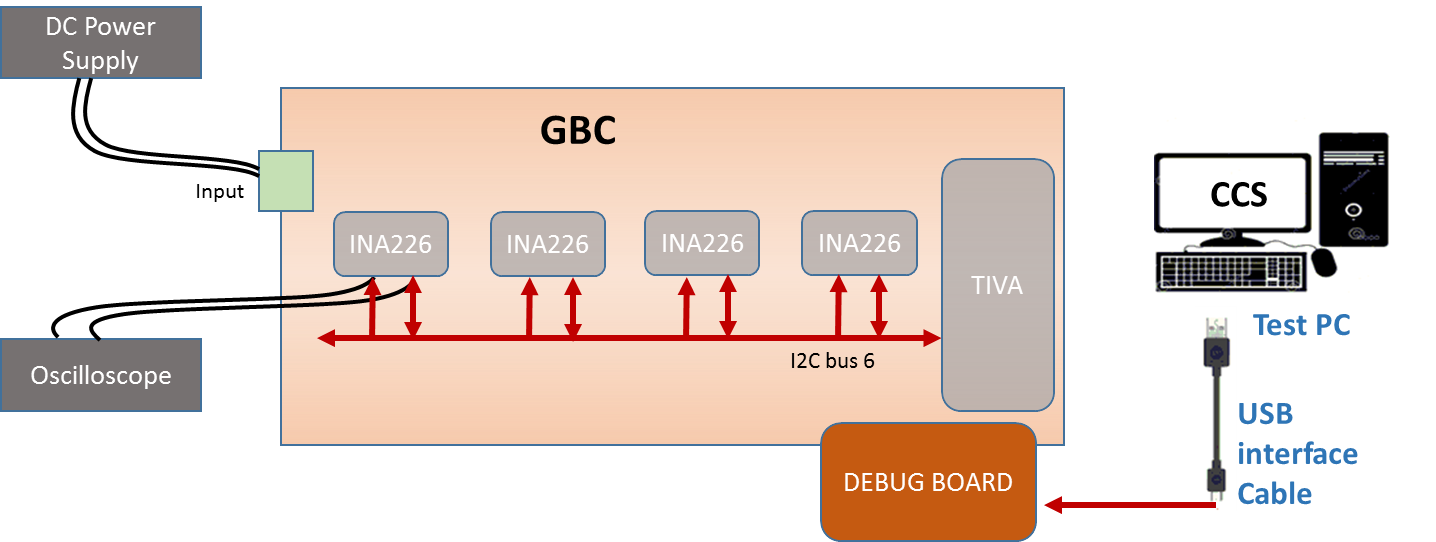
1. Connect Debug board to GBC board to flash the code.
2. Connect a Test PC with CCS to debug board.
3. Import the code in Code Composer Studio.
4. Configure DC power supply to give a voltage of 18V.
5. Run the code in CCS.
6. Validate the output as per the above requirement.

##### **Reference**

Further details can be found in Page 45 and 46 of GBC schematic Life-2.

### Power Monitor – I2C (INA226)

#### Test Setup



**Figure 38. Power Monitor I2C - Test Setup Diagram**

#### Test Case: Electrical Validation (Test ID: TIV.3.1)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the electrical characteristics of I2C interface of Power monitor IC.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | Failure of this test case will result in improper load current and power readings. |
| Compliance | NA |  |

**Table 292. Impact of Failure of EV – Power Monitor I2C**

1. **Measurement Locations**

U185.5, U185.4

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50µs

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board

##### **Software Requisites**

1. Code Composer Studio Tool
2. Tiva-power monitor I2C code

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 293. Test Condition for EV – Power Monitor I2C**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| TIVA\_PWRMNTR\_I2C6\_SCLK | U185.5 | VLOW (max) (V) | -0.5 | 0.99 |
| VHIGH (min) (V) | 2.31 | 6 |
| Rise time (ns) | 0 | 1000 |
| Fall time (ns) | 0 | 300 |
| Frequency (kHz) | 0 | 100 |
| TIVA\_PWRMNTR\_I2C6\_SDA | U185.4 | VLOW (max) (V) | -0.5 | 0.99 |
| VHIGH (min) (V) | 2.31 | 6 |
| Rise time (ns) | 0 | 1000 |
| Fall time (ns) | 0 | 300 |

**Table 294. Requirements for EV – Power Monitor I2C**

##### **Test Procedure**

1. Connect Debug board to GBC board to flash the code.
2. Connect a Test PC with CCS to debug board.
3. Import the code in Code Composer Studio.
4. Configure DC power supply to give a voltage of 18V.
5. Probe the I2C signal at U185.5 (SCL), U185.4 (SDA).
6. Run the code in CCS.
7. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 21, 28, 55, 60 and 75 of GBC schematic Ver. Life-2.

#### Test Case: Signal Integrity (Test ID: TIV.3.2)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the signal integrity of I2C interface of Power monitor IC.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | Failure of this test case will result in improper load current and power readings. |
| Compliance | NA |  |

**Table 295. Impact of Failure of SI– Power Monitor I2C**

1. **Measurement Locations**

U185.5, U185.4

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50µs

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board

##### **Software Requisites**

1. Code Composer Studio Tool
2. Tiva-power monitor I2C code

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 296. Test Condition for SI – Power Monitor I2C**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| TIVA\_PWRMNTR\_I2C6\_SCLK | U185.5 | Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |
| TIVA\_PWRMNTR\_I2C6\_SDA | U185.4 | data set-up time (ns) | 250 | 10000 |
| data hold time (ns) | 300 | 10000 |
| Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |

**Table 297. Requirements for SI – Power Monitor I2C**

##### **Test Procedure**

1. Connect Debug board to GBC board to flash the code.
2. Connect a Test PC with CCS to debug board.
3. Import the code in Code Composer Studio.
4. Configure DC power supply to give a voltage of 18V.
5. Probe the I2C signal at U185.5 (SCL), U185.4 (SDA).
6. Run the code in CCS.
7. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 21, 28, 55, 60 and 75 of GBC schematic Ver. Life-2.

#### Test Case: Functional Validation (Test ID: TIV.3.3)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the I2C interface of Power monitor IC.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Registers of the power monitor IC become inaccessible on failure of this test case. |
| Performance | NA |  |
| Compliance | NA |  |
|  |  |  |

**Table 298. Impact of Failure of FV – Power Monitor I2C**

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board

##### **Software Requisites**

1. Code Composer Studio Tool
2. Tiva-power monitor I2C code

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 299. Test Condition for FV – Power Monitor I2C**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| I2C Interface | Manufacture ID | Read Manufacture ID, 5449 from Address FEh |

**Table 300. Requirements for FV – Power Monitor I2C**

##### **Test Procedure**

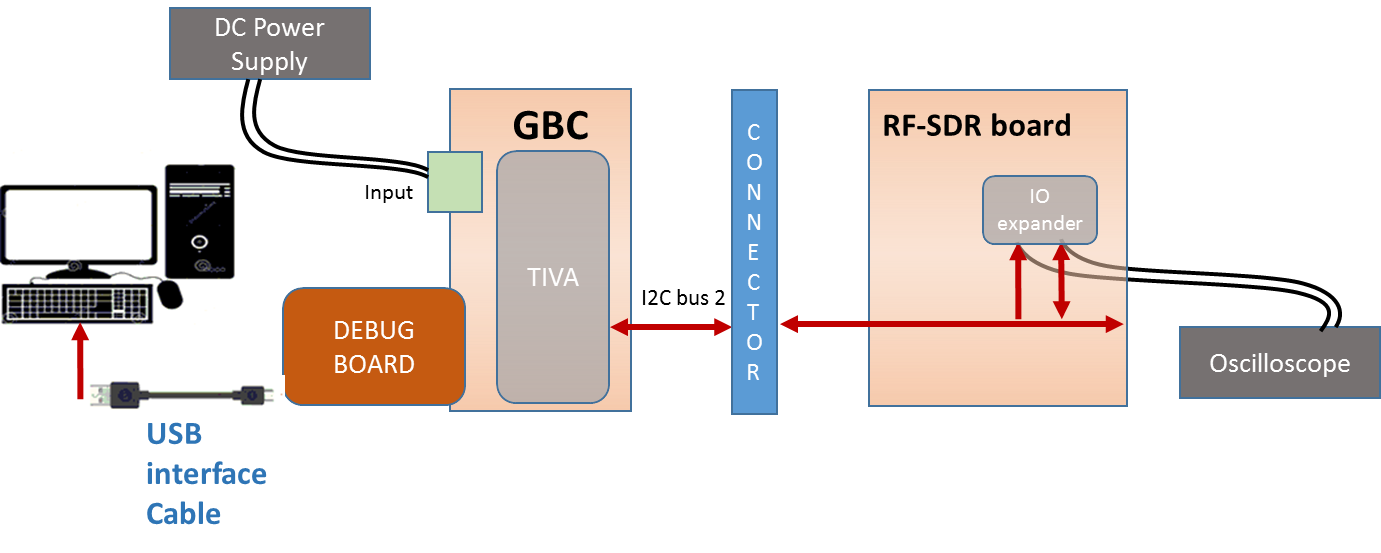
1. Connect Debug board to GBC board to flash the code.
2. Connect a Test PC with CCS to Debug board.
3. Import the code in Code Composer Studio.
4. Configure DC power supply to give a voltage of 18V.
5. Run the code in CCS.
6. Validate the output as per the above requirement.

##### **Reference**

Further details can be found in Page 21, 28, 55, 60 and 75 of GBC schematic Ver. Life-2.

### RF-SDR board – I2C (PCA9557PW, 118)

#### Test Setup



**Figure 39. RF-SDR board I2C - Test Setup Diagram**

#### Test Case: Electrical Validation (Test ID: TIV.4.1)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the electrical characteristics of I2C interface of IO expander in RF-SDR board.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | Failure of this test case will result in improper data from IO expander. |
| Compliance | NA |  |

**Table 301. Impact of Failure of EV – RF-SDR board I2C**

1. **Measurement Locations**

R1089.2/ R1088.2, R2034/ R2033 (RF-SDR board)

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50µs

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. RF-SDR board

##### **Software Requisites**

1. Code Composer Studio Tool
2. Tiva-IO expander (RF-SDR board) I2C code

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 302. Test Condition for EV – RF-SDR board I2C**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| **Before Level Shifter** | | | | |
| TIVA\_TRXFECONN\_I2C2\_SCLK | R1089.2 | VLOW (max) (V) | -0.5 | 0.99 |
| VHIGH (min) (V) | 2.31 | 5.5 |
| Rise time (ns) | 0 | 300 |
| Fall time (ns) | 0 | 300 |
| Frequency (kHz) | 0 | 400 |
| TIVA\_TRXFECONN\_I2C2\_SDA | R1088.2 | VLOW (max) (V) | -0.5 | 0.99 |
| VHIGH (min) (V) | 2.31 | 5.5 |
| Rise time (ns) | 0 | 300 |
| Fall time (ns) | 0 | 300 |
| **After Level Shifter** | | | | |
| SYS\_I2C\_2\_SCL | R2034 | VLOW (max) (V) | -0.5 | 0.99 |
| VHIGH (min) (V) | 2.31 | 5.5 |
| Rise time (ns) | 0 | 300 |
| Fall time (ns) | 0 | 300 |
| Frequency (kHz) | 0 | 400 |
| SYS\_I2C\_2\_SDA | R2033 | VLOW (max) (V) | -0.5 | 0.99 |
| VHIGH (min) (V) | 2.31 | 5.5 |
| Rise time (ns) | 0 | 300 |
| Fall time (ns) | 0 | 300 |

**Table 303. Requirements for EV – RF-SDR board I2C**

##### **Test Procedure**

1. Connect RF-SDR board to GBC board.
2. Connect Debug board to GBC board to flash the code.
3. Connect a Test PC with CCS to debug board.
4. Import the code in Code Composer Studio.
5. Configure DC power supply to give a voltage of 18V.
6. Probe the I2C signal at R1089.2 (SCL), R1088.2 (SDA) for before level shifter and R2034 (SCL), R2033 (SDA) for after level shifter.
7. Run the code in CCS.
8. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 60 and 73 and page 76 of GBC schematic Ver. Life-2 and page 44 of RF-SDR board schematic Ver. Life-2.

#### Test Case: Signal Integrity (Test ID: TIV.4.2)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the signal integrity of IO expander in RF-SDR board.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | Failure of this test case will result in improper data from IO expander. |
| Compliance | NA |  |

**Table 304. Impact of Failure of SI – RF-SDR board I2C**

1. **Measurement Locations**

R1089.2/ R1088.2, R2034/ R2033 (RF-SDR board)

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50µs

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. RF-SDR board

##### **Software Requisites**

1. Code Composer Studio Tool
2. Tiva-IO expander (RF-SDR board) I2C code

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 305. Test Condition for SI – RF-SDR board I2C**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| **Before Level Shifter** | | | | |
| TIVA\_TRXFECONN\_I2C2\_SCLK | R1089.2 | Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |
| TIVA\_TRXFECONN\_I2C2\_SDA | R1088.2 | data set-up time (ns) | 100 | 2500 |
| data hold time (ns) | 300 | 2500 |
| Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |
| **After Level Shifter** | | | | |
| SYS\_I2C\_2\_SCL | R2034 | Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |
| SYS\_I2C\_2\_SDA | R2033 | data set-up time (ns) | 100 | 2500 |
| data hold time (ns) | 300 | 2500 |
| Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |

**Table 306. Requirements for SI – RF-SDR board I2C**

##### **Test Procedure**

1. Connect RF-SDR board to GBC board.
2. Connect Debug board to GBC board to flash the code.
3. Connect a Test PC with CCS to debug board.
4. Import the code in Code Composer Studio.
5. Configure DC power supply to give a voltage of 18V.
6. Probe the I2C signal at R1089.2 (SCL), R1088.2 (SDA) for before level shifter and R2034 (SCL), R2033 (SDA) for after level shifter.
7. Run the code in CCS.
8. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 60 and 73 and page 76 of GBC schematic Ver. Life-2 and page 44 of RF-SDR board schematic Ver. Life-2.

#### Test Case: Functional Validation (Test ID: TIV.4.3)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the I2C interface of IO expander in RF-SDR board.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Registers of the IO expander become inaccessible on failure of this test case. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 307. Impact of Failure of FV – RF-SDR board I2C**

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. RF-SDR board

##### **Software Requisites**

1. Code Composer Studio Tool
2. Tiva-IO expander (RF-SDR board) I2C code

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 308. Test Condition for FV – RF-SDR board I2C**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| I2C Interface | Input register data | Register 0x3 written with value 0xfe (slave address 0x1b)  or  Register 0x1 written with value 0xaa (slave address 0x1e) |

**Table 309. Requirements for FV – RF-SDR board I2C**

##### **Test Procedure**

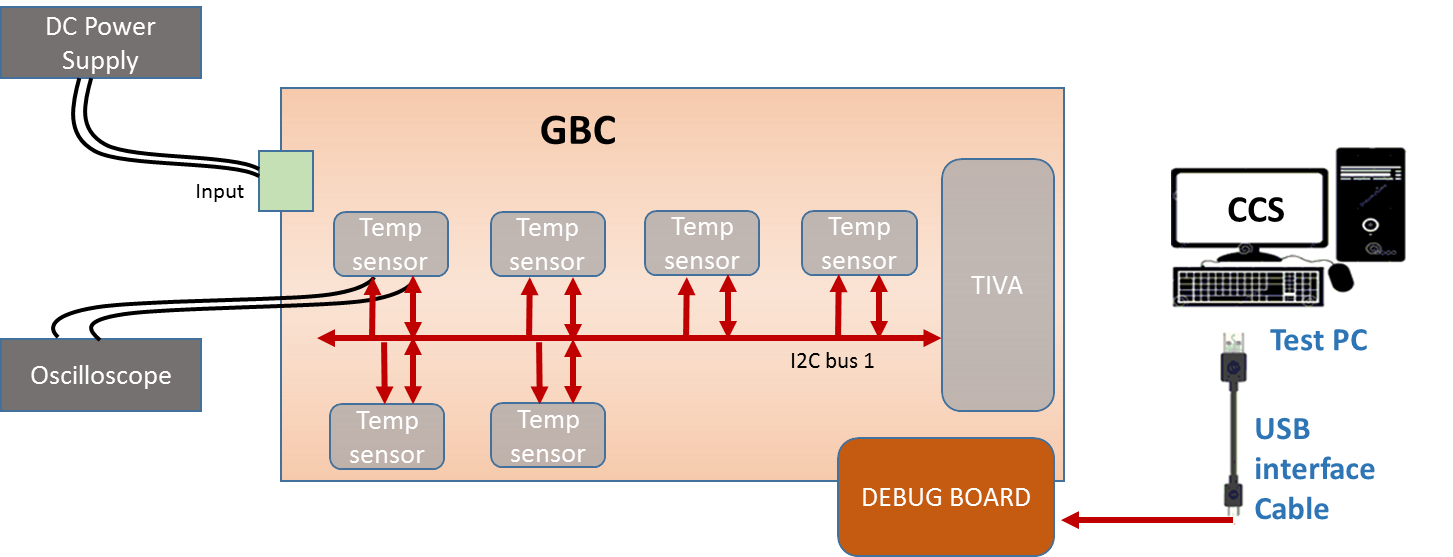
1. Connect RF-SDR board to GBC board.
2. Connect Debug board to GBC board to flash the code.
3. Connect a Test PC with CCS to debug board.
4. Import the code in Code Composer Studio.
5. Configure DC power supply to give a voltage of 18V.
6. Run the code in CCS.
7. Validate the output as per the above requirement.

##### **Reference**

Further details can be found in Page 60 and 73 and page 76 of GBC schematic Ver. Life-2 and page 44 of RF-SDR board schematic Ver. Life-2.

### Temp Sensor – I2C (SE98ATP, 547)

#### Test Setup



**Figure 40. Temp Sensor I2C - Test Setup Diagram**

#### Test Case: Electrical Validation (Test ID: TIV.5.1)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the electrical characteristics of I2C interface of temperature sensor.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | Failure of this test case will result in improper temperature readings. |
| Compliance | NA |  |

**Table 310. Impact of Failure of EV – Temp Sensor I2C**

1. **Measurement Locations**

R10255.2/ R10256.2, R10221.2/ R10222.2

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50µs

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board

##### **Software Requisites**

1. Code Composer Studio Tool
2. Tiva-temperature sensor I2C code

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 311. Test Condition for EV – Temp Sensor I2C**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| **U215 (Near Tiva)** | | | | |
| TIVA\_TEMPSEN\_I2C1\_SCLK | R10255.2 | VLOW (max) (V) | -0.5 | 0.99 |
| VHIGH (min) (V) | 2.31 | 4.3 |
| Rise time (ns) | 0 | 1000 |
| Fall time (ns) | 0 | 300 |
| Frequency (kHz) | 0 | 100 |
| TIVA\_TEMPSEN\_I2C1\_SDA | R10256.2 | VLOW (max) (V) | -0.5 | 0.99 |
| VHIGH (min) (V) | 2.31 | 4.3 |
| Rise time (ns) | 0 | 1000 |
| Fall time (ns) | 0 | 300 |
| **U210 (Far from Tiva)** | | | | |
| TIVA\_TEMPSEN\_I2C1\_SCLK | R10221.2 | VLOW (max) (V) | -0.5 | 0.99 |
| VHIGH (min) (V) | 2.31 | 4.3 |
| Rise time (ns) | 0 | 1000 |
| Fall time (ns) | 0 | 300 |
| Frequency (kHz) | 0 | 100 |
| TIVA\_TEMPSEN\_I2C1\_SDA | R10222.2 | VLOW (max) (V) | -0.5 | 0.99 |
| VHIGH (min) (V) | 2.31 | 4.3 |
| Rise time (ns) | 0 | 1000 |
| Fall time (ns) | 0 | 300 |

**Table 312. Requirements for EV – Temp Sensor I2C**

##### **Test Procedure**

1. Connect Debug board to GBC board to flash the code.
2. Connect a Test PC with CCS to debug board.
3. Import the code in Code Composer Studio.
4. Configure DC power supply to give a voltage of 18V.
5. Probe the I2C signal at R10255.2 (SCL), R10256.2 (SDA) for near Tiva and R10221.2 (SCL), R10222.2 (SDA) for far from Tiva.
6. Run the code in CCS.
7. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 70 and 71 of GBC schematic Ver. Life-2.

#### Test Case: Signal Integrity (Test ID: TIV.5.2)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the signal integrity of I2C interface of temperature sensor.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | Failure of this test case will result in improper temperature readings. |
| Compliance | NA |  |

**Table 313. Impact of Failure of SI – Temp Sensor I2C**

1. **Measurement Locations**

R10255.2/ R10256.2, R10221.2/ R10222.2

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50µs

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board

##### **Software Requisites**

1. Code Composer Studio Tool
2. Tiva-temperature sensor I2C code

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 314. Test Condition for SI – Temp Sensor I2C**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| **U215 (Near Tiva)** | | | | |
| TIVA\_TEMPSEN\_I2C1\_SCLK | R10255.2 | Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |
| TIVA\_TEMPSEN\_I2C1\_SDA | R10256.2 | data set-up time (ns) | 250 | 10000 |
| data hold time (ns) | 200 | 3450 |
| Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |
| **U210 (Far from Tiva)** | | | | |
| TIVA\_TEMPSEN\_I2C1\_SCLK | R10221.2 | Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |
| TIVA\_TEMPSEN\_I2C1\_SDA | R10222.2 | data set-up time (ns) | 250 | 10000 |
| data hold time (ns) | 200 | 3450 |
| Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |

**Table 315. Requirements for SI – Temp Sensor I2C**

##### **Test Procedure**

1. Connect Debug board to GBC board to flash the code.
2. Connect a Test PC with CCS to Debug board.
3. Import the code in Code Composer Studio.
4. Configure DC power supply to give a voltage of 18V.
5. Probe the I2C signal at R10255.2 (SCL), R10256.2 (SDA) for near Tiva and R10221.2 (SCL), R10222.2 (SDA) for far from Tiva.
6. Run the code in CCS.
7. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 70 and 71 of GBC schematic Ver. Life-2.

#### Test Case: Functional Validation (Test ID: TIV.5.3)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the I2C interface of temperature sensor.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Registers of the temperature sensor become inaccessible on failure of this test case. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 316. Impact of Failure of FV – Temp Sensor I2C**

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board

##### **Software Requisites**

1. Code Composer Studio Tool
2. Tiva-temperature sensor I2C code

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 317. Test Condition for FV – Temp Sensor I2C**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| I2C Interface | 1. Device ID 2. Manufacture ID | 1. Register 0x6 is read with 0x1131. 2. Register 0x7 is read with 0xa102. |

**Table 318. Requirements for FV – Temp Sensor I2C**

##### **Test Procedure**

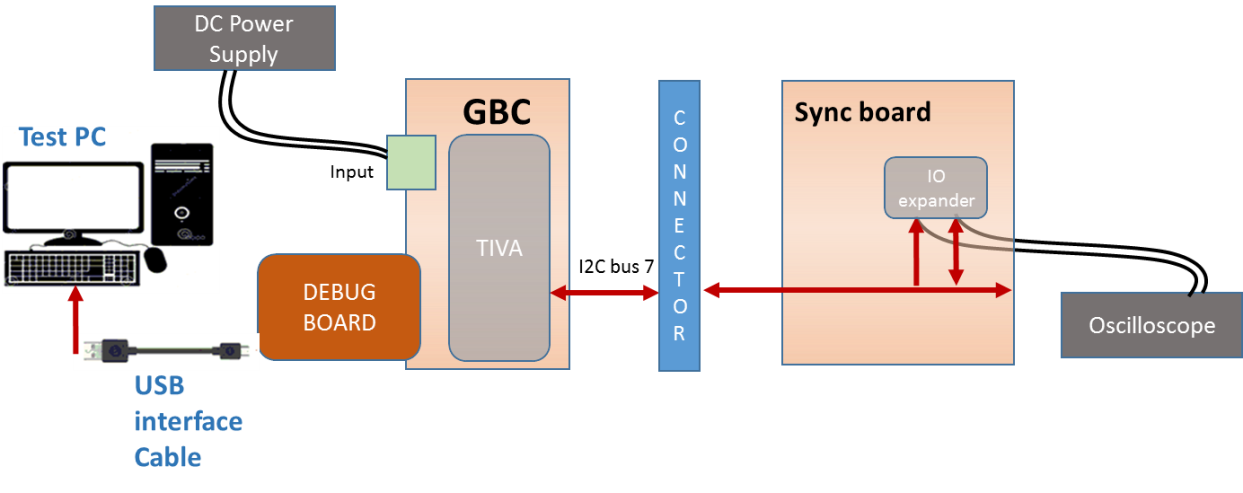
1. Connect Debug board to GBC board to flash the code.
2. Connect a Test PC with CCS to Debug board.
3. Import the code in Code Composer Studio.
4. Configure DC power supply to give a voltage of 18V.
5. Run the code in CCS.
6. Validate the output as per the above requirement.

##### **Reference**

Further details can be found in Page 70 and 71 of GBC schematic Ver. Life-2.

### Sync board – I2C (PCA9557PW, 118)

#### Test Setup



**Figure 41. Sync board I2C - Test Setup Diagram**

#### Test Case: Electrical Validation (Test ID: TIV.6.1)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the electrical characteristics of I2C interface of IO expander in sync board.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | Failure of this test case will result in improper data from IO expander. |
| Compliance | NA |  |

**Table 319. Impact of Failure of EV – Sync board I2C**

1. **Measurement Locations**

U1.1, U1.2 (Sync board)

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50µs

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Sync board

##### **Software Requisites**

1. Code Composer Studio Tool
2. Tiva-IO expander (Sync board) I2C code

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 320. Test Condition for EV – Sync board I2C**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| TIVA\_SYNCCONN\_I2C7\_SCLK | U1.1 | VLOW (max) (V) | -0.5 | 0.99 |
| VHIGH (min) (V) | 2.31 | 5.5 |
| Rise time (ns) | 0 | 1000 |
| Fall time (ns) | 0 | 300 |
| Frequency (kHz) | 0 | 100 |
| TIVA\_SYNCCONN\_I2C7\_SDA | U1.2 | VLOW (max) (V) | -0.5 | 0.99 |
| VHIGH (min) (V) | 2.31 | 5.5 |
| Rise time (ns) | 0 | 1000 |
| Fall time (ns) | 0 | 300 |

**Table 321. Requirements for EV – Sync board I2C**

##### **Test Procedure**

1. Connect Sync board to GBC board.
2. Connect Debug board to GBC board to flash the code.
3. Connect a Test PC with CCS to Debug board.
4. Import the code in Code Composer Studio.
5. Configure DC power supply to give a voltage of 18V.
6. Probe the I2C signal at U1.1 (SCL), U1.2 (SDA).
7. Run the code in CCS.
8. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 60 and 74 of GBC schematic Ver. Life-2 and page 4 of Sync board schematic Life-1.

#### Test Case: Signal Integrity (Test ID: TIV.6.2)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the signal integrity of IO expander in sync board.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | Failure of this test case will result in improper data from IO expander. |
| Compliance | NA |  |

**Table 322. Impact of Failure of SI – Sync board I2C**

1. **Measurement Locations**

U1.1, U1.2 (Sync board)

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50µs

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Sync board

##### **Software Requisites**

1. Code Composer Studio Tool
2. Tiva-IO expander (Sync board) I2C code

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 323. Test Condition for SI – Sync board I2C**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| TIVA\_SYNCCONN\_I2C7\_SCLK | U1.1 | Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |
| TIVA\_SYNCCONN\_I2C7\_SDA | U1.2 | data set-up time (ns) | 250 | 10000 |
| data hold time (ns) | 300 | 10000 |
| Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |

**Table 324. Requirements for SI – Sync board I2C**

##### **Test Procedure**

1. Connect Sync board to GBC board.
2. Connect Debug board to GBC board to flash the code.
3. Connect a Test PC with CCS to Debug board.
4. Import the code in Code Composer Studio.
5. Configure DC power supply to give a voltage of 18V.
6. Probe the I2C signal at U1.1 (SCL), U1.2 (SDA).
7. Run the code in CCS.
8. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 60 and 74 of GBC schematic Ver. Life-2 and page 4 of Sync board schematic Life-1.

#### Test Case: Functional Validation (Test ID: TIV.6.3)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the I2C interface of IO expander in sync board.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Registers of the IO expander become inaccessible on failure of this test case. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 325. Impact of Failure of FV – Sync board I2C**

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. Sync board

##### **Software Requisites**

1. Code Composer Studio Tool
2. Tiva-IO expander (Sync board) I2C code

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 326. Test Condition for FV – Sync board I2C**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| I2C Interface | Input register data | Register 0x3 written with value 0x1f |

**Table 327. Requirements for FV – Sync board I2C**

##### **Test Procedure**

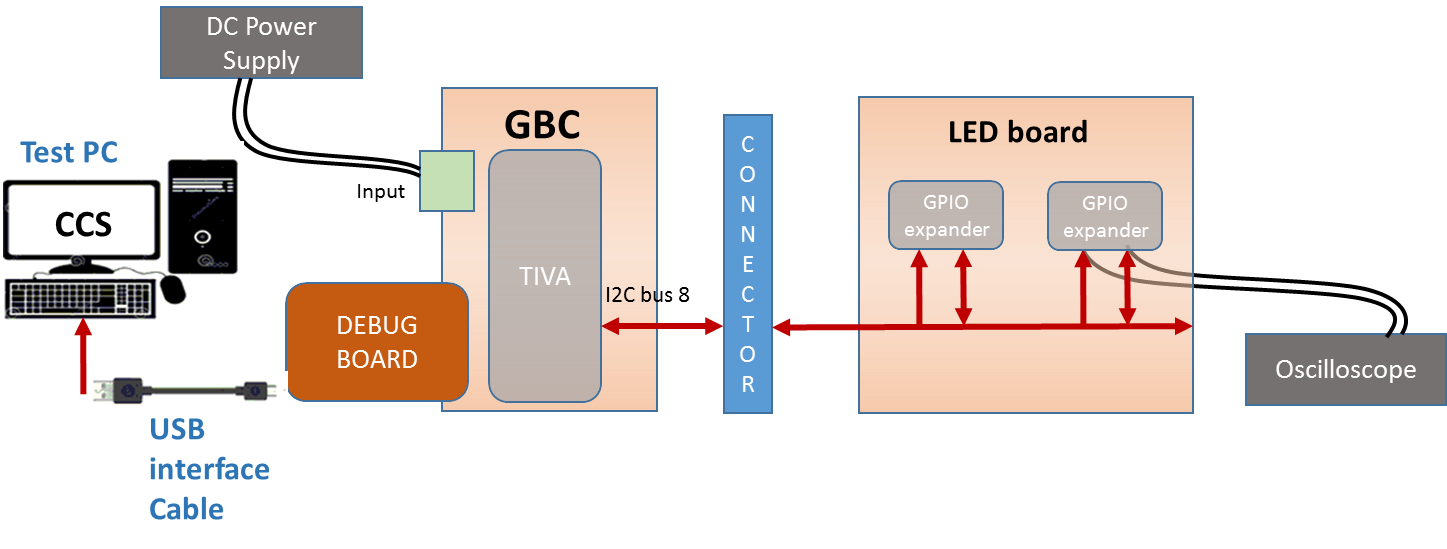
1. Connect Sync board to GBC board.
2. Connect Debug board to GBC board to flash the code.
3. Connect a Test PC with CCS to debug board.
4. Import the code in Code Composer Studio.
5. Configure DC power supply to give a voltage of 18V.
6. Run the code in CCS.
7. Validate the output as per the above requirement.

##### **Reference**

Further details can be found in Page 60 and 74 of GBC schematic Ver. Life-2 and page 4 of Sync board schematic RevLife-1A.

### LED board – I2C (SX1509BIULTRT)

#### Test Setup



**Figure 42. LED board I2C - Test Setup Diagram**

#### Test Case: Electrical Validation (Test ID: TIV.7.1)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the electrical characteristics of I2C interface of GPIO expander in LED board.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | Failure of this test case will result in improper data from GPIO expander. |
| Compliance | NA |  |

**Table 328. Impact of Failure of EV – LED board I2C**

1. **Measurement Locations**

U1.25, U1.24 (LED board)

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50µs

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. LED board

##### **Software Requisites**

1. Code Composer Studio Tool
2. Tiva-GPIO expander (LED board) I2C code

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 329. Test Condition for EV – LED board I2C**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| LED\_I2C\_SCL | U1.25 | VLOW (max) (V) | -0.4 | 0.99 |
| VHIGH (min) (V) | 2.31 | 3.3 |
| Rise time (ns) | 0 | 1000 |
| Fall time (ns) | 0 | 300 |
| Frequency (kHz) | 0 | 100 |
| LED\_I2C\_SDA | U1.24 | VLOW (max) (V) | -0.4 | 0.99 |
| VHIGH (min) (V) | 2.31 | 3.3 |
| Rise time (ns) | 0 | 1000 |
| Fall time (ns) | 0 | 300 |

**Table 330. Requirements for EV – LED board I2C**

##### **Test Procedure**

1. Connect LED board to GBC board.
2. Connect Debug board to GBC board to flash the code.
3. Connect a Test PC with CCS to Debug board.
4. Import the code in Code Composer Studio.
5. Configure DC power supply to give a voltage of 18V.
6. Probe the I2C signal at U1.25 (SCL), U1.24 (SDA).
7. Run the code in CCS.
8. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 46 and 87 of GBC schematic Ver. Life-2 and Page 1 the LED schematic Ver. Life-2.

#### Test Case: Signal Integrity (Test ID: TIV.7.2)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the signal integrity of GPIO expander in LED board.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | NA |  |
| Performance | Yes | Failure of this test case will result in improper data from GPIO expander. |
| Compliance | NA |  |

**Table 331. Impact of Failure of SI – LED board I2C**

1. **Measurement Locations**

U1.25, U1.24 (LED board)

##### **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50µs

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. LED board

##### **Software Requisites**

1. Code Composer Studio Tool
2. Tiva-GPIO expander (LED board) I2C code

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 332. Test Condition for SI – LED board I2C**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| LED\_I2C\_SCL | U1.25 | Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |
| LED\_I2C\_SDA | U1.24 | data set-up time (ns) | 250 | 10000 |
| data hold time (ns) | 300 | 10000 |
| Positive Over-shoot (V) | 0 | 0.33 |
| Negative Over-shoot (V) | 0 | 0.33 |

**Table 333. Requirements for SI – LED board I2C**

##### **Test Procedure**

1. Connect LED board to GBC board.
2. Connect Debug board to GBC board to flash the code.
3. Connect a Test PC with CCS to debug board.
4. Import the code in Code Composer Studio.
5. Configure DC power supply to give a voltage of 18V.
6. Probe the I2C signal at U1.25 (SCL), U1.24 (SDA).
7. Run the code in CCS.
8. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 46 and 87 of GBC schematic Ver. Life-2 and Page 1 the LED schematic Ver. Life-2.

#### Test Case: Functional Validation (Test ID: TIV.7.3)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the I2C interface of GPIO expander in LED board.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Registers of the gpio expander become inaccessible on failure of this test case. |
| Performance | NA |  |
| Compliance |  |  |

**Table 334. Impact of Failure of FV – LED board I2C**

##### **Test Equipment List**

1. DC power supply: E3633A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. LED board

##### **Software Requisites**

1. Code Composer Studio Tool
2. Tiva-GPIO expander (LED board) I2C code

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 335. Test Condition for FV – LED board I2C**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| I2C Interface | 1. REG\_CLOCK 2. REG\_MISC | Slave: 3e   1. REG\_CLOCK: 0x0 2. REG\_MISC: 0x24 |

**Table 336. Requirements for FV– LED board I2C**

##### **Test Procedure**

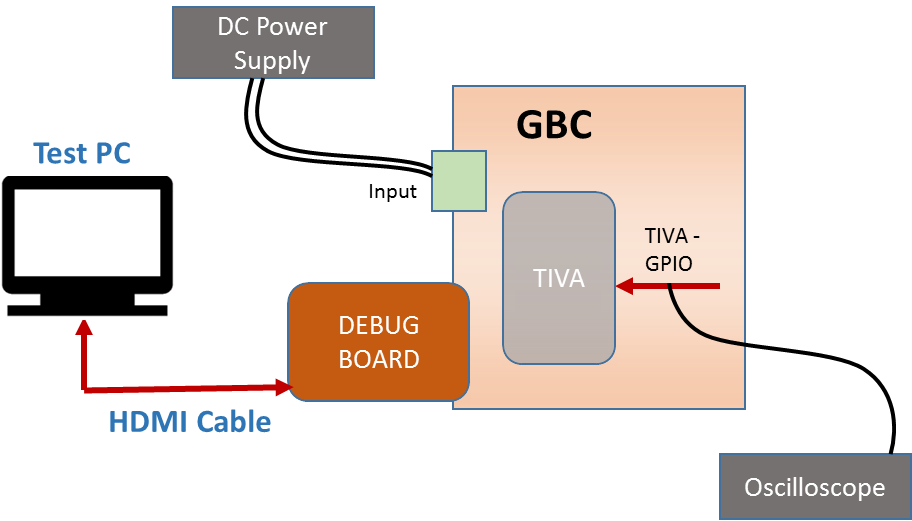
1. Connect LED board to GBC board.
2. Connect Debug board to GBC board to flash the code.
3. Connect a Test PC with CCS to debug board.
4. Import the code in Code Composer Studio.
5. Configure DC power supply to give a voltage of 18V.
6. Run the code in CCS.
7. Validate the output as per the above requirement.

##### **Reference**

Further details can be found in Page 46 and 87 of GBC schematic Ver. Life-2 and Page 1 the LED schematic Ver. Life-2.

### TIVA GPIO

#### Test Setup



**Figure 43. TIVA GPIO - Test Setup Diagram**

* + - 1. **Test Case:Control inputs functional validation *(Test ID: TIV.10.1)*** 
         1. **Description**

1. **Purpose**The purpose of the test case is to execute the control inputs functional validation of TIVA- GPIO signals.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case will cause the GPIO lines to not toggle and hence not work as per design. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 337. Impact of Failure of Control inputs FV – TIVA GPIO**

* + - * 1. **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A
   * + - 1. **Equipment Settings**
3. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50ms

* + - * 1. **Hardware Requisites**

1. GBC board
   * + - 1. **Software Requisites**

NA

* + - * 1. **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 338. Test Condition for Control inputs FV – TIVA GPIO**

* + - * 1. **DUT Settings**

NA

* + - * 1. **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| Control inputs functional validation | Toggling of TIVA - GPIO signals | Toggle the GPIO lines which are input to TIVA through hardware. GPIO lines should toggle between High and Low voltages. |

**Table 339. Requirements for Control inputs FV – TIVA GPIO**

* + - * 1. **Test Procedure**

1. Configure DC power supply to give a voltage of 18V.
2. Toggling the GPIO lines which are input to TIVA through hardware in GBC board.
3. Validate the output as per the above requirement.
   * + - 1. **Reference**

Further details can be found in Page 60 of GBC schematic Life-2.

### TIVA GPIO

#### Test Setup



**Figure 44. TIVA GPIO - Test Setup Diagram**

* + - 1. **Test Case:Control outputs functional validation *(Test ID: TIV.11.1)*** 
         1. **Description**

1. **Purpose**The purpose of the test case is to execute the control outputs functional validation of TIVA- GPIO signals.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case will cause the GPIO lines to not toggle and hence not work as per design. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 340. Impact of Failure of Control outputs FV – TIVA GPIO**

* + - * 1. **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A
   * + - 1. **Equipment Settings**
3. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50ms

* + - * 1. **Hardware Requisites**

1. GBC board
2. Debug board
   * + - 1. **Software Requisites**
3. Code Composer Studio Tool
4. Tiva-GPIO code
   * + - 1. **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 341. Test Condition for Control outputs FV – TIVA GPIO**

* + - * 1. **DUT Settings**

NA

* + - * 1. **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| Control outputs functional validation | Toggling of TIVA - GPIO signals | Toggle the GPIO lines which are output from TIVA by software control. GPIO lines should toggle between High and Low voltages. |

**Table 342. Requirements for Control outputs FV – TIVA GPIO**

* + - * 1. **Test Procedure**

1. Connect Debug board to GBC board to flash the code.
2. Connect a Test PC with CCS to debug board.
3. Import the code in Code Composer Studio.
4. Configure DC power supply to give a voltage of 18V.
5. Probe the GPIO signals.
6. Run the code in CCS.
7. Validate the output as per the above requirement.
   * + - 1. **Reference**

Further details can be found in Page 60 of GBC schematic Life-2.

### ETH SW MGMT Interface

* + - 1. **Test Case: *Functional Validation (Test ID: TIV.12.1)*** 
         1. **Description**

1. **Purpose**The purpose of the test case is to validate the TIVA in order to control and configure the Marvell switch.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Failure of this test case will not able to route MDI signals across modules / devices. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 343. Impact of Failure of ETH SW MGMT Interface**

* + - * 1. **Test Equipment List**

1. Oscilloscope: MSO9404A
2. DC power supply: E3633A
   * + - 1. **Equipment Settings**
3. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

1. Oscilloscope: MSO9404A

Voltage per division: 1V

Time scale: 50ms

* + - * 1. **Hardware Requisites**

1. GBC board
2. Debug board
   * + - 1. **Software Requisites**
3. Code Composer Studio Tool
4. Tiva-Marvell code
   * + - 1. **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 344. Test Condition for ETH SW MGMT Interface**

* + - * 1. **DUT Settings**

NA

* + - * 1. **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| Functional validation | Reading Device ID | Able to read Device ID – 0X0141 |

**Table 345. Requirements for ETH SW MGMT Interface**

* + - * 1. **Test Procedure**

1. Connect Debug board to GBC board to flash the code.
2. Connect a Test PC with CCS to debug board.
3. Import the code in Code Composer Studio.
4. Configure DC power supply to give a voltage of 18V.
5. Run the code in CCS.
6. TIVA uses GPIO bit banging method to control and configure the Marvell switch as there is no dedicated MDIO module in TM4c1294NCPDT controller
7. Read SMI register values including fixed Device ID registers
8. Validate the output as per the above requirement.
   * + - 1. **Reference**

Further details can be found in Page 56 and 60 of GBC schematic Life-2.

# Ethernet

## Test Purpose and Description

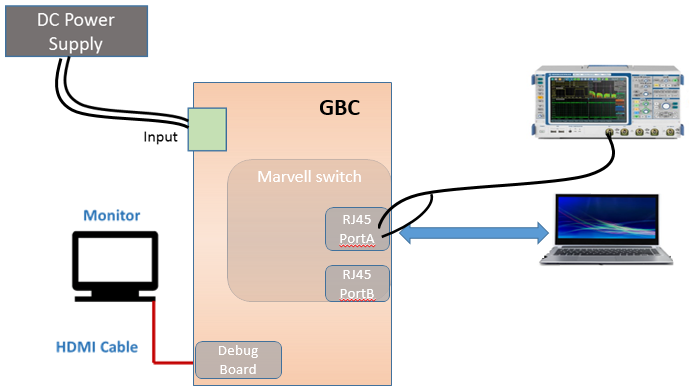
The GBC board shall provide an Ethernet switch for providing Ethernet connectivity between Port A, Port B, Main processor, housekeeping microcontroller, for transferring IQ samples and provision for future adaptor board containing IEEE1588 PTP processor.

## Ethernet Sub-system constitutes of below components

1. PoE(PD) – MDI
2. TIVA Ethernet

### PoE *(PD) - MDI*

#### Test Setup



**Figure 45.INTEL POE (PD) - MDI - Test Setup Diagram**

#### Test Case: Electrical validation (Test ID: ETH.1.1)

##### **Description**

1. **Purpose**The purpose of this test case is to verify MDI signal characteristics (Interface between Marvell Switch (88E6071) to POE PD port. (PORT A)
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Packet loss and data inconsistency |
| Performance | Yes | Data transfer will be affected |
| Compliance | NA |  |

**Table 346. Impact of Failure of EV – POE (PD) - MDI**

1. **Measurement Locations**

J1A.1, J1A.2, J1A.3 and J1A.6

##### **Test Equipment List**

1. Oscilloscope: DPO7354C
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: DPO7354C

Voltage per division: 500mV

Time scale: 50ns

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. HDMI Monitor

##### **Software Requisites**

1. Ethernet driver
2. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 347. Test Condition for EV – POE (PD) - MDI**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| LANSW\_ETHSW\_P1\_TXP **/** TXN **(**From Port to Switch) | | | | |
| TXP  TXN | J1A.1  J1A.2 | Vp-p (V) | 1.9 | 2.63 |
| Overshoot (%) | 0 | 10 |
| Undershoot (%) | 0 | 10 |
| Data rate (Mbps) |  | 100 |
| ETHSW\_LANSW\_P1\_RXP **/** RXN **(**From Switch to Port) | | | | |
| RXP  RXN | J1A.3  J1A.6 | Vp-p (V) | 1.9 | 2.63 |
| Overshoot (%) | 0 | 10 |
| Undershoot (%) | 0 | 10 |
| Data rate (Mbps) |  | 100 |

**Table 348. Requirements for EV – POE (PD) - MDI**

##### **Test Procedure**

1. Connect Debug board to GBC board with OS and Ethernet driver installed
2. Connect a monitor to debug board using HDMI cable
3. Connect a Linux PC to port A of GBC board.
4. Configure DC power supply to give a voltage of 18V.
5. Assign static IP address at both GBC and Linux PC.
6. Establish communication by pinging each other.
7. The MDI transmit signals (from Port to Switch) are measured at J1A.1 (TXP) and J1A.2 (TXN).
8. The MDI receiving signals (from Switch to Port) are measured at J1A.3 (RXP) and J1A.6 (RXN).
9. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 41, 56 and 57 of GBC schematic Life-2.

#### Test Case: Functional Validation (Test ID: ETH.1.2)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the function of POE (PD)-MDI.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Registers of SOC become inaccessible on failure of this test case and data transfer can be affected. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 349. Impact of Failure of FV – POE (PD) MDI**

##### **Test Equipment List**

1. Oscilloscope: DPO7354C
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: DPO7354C

Voltage per division: 500mV

Time scale: 50ns

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. HDMI Monitor

##### **Software Requisites**

1. Ethernet driver
2. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 350. Test Condition of FV – POE (PD) MDI**

##### **DUT Settings**

NA.

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| Ethernet Interface | IP Address | Ping each other using static IP address and ensure the data transfer with no packet loss |

**Table 351. Requirements for FV – POE (PD) MDI**

##### **Test Procedure**

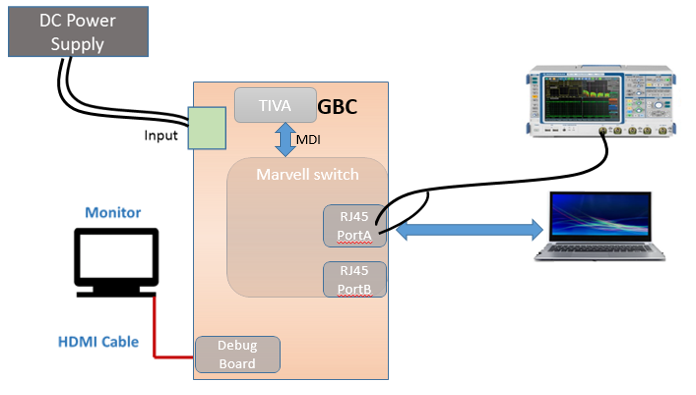
1. Connect Debug board to GBC board with OS and Ethernet driver installed
2. Connect a monitor to debug board using HDMI cable
3. Connect a Linux PC to port A of GBC board.
4. Configure DC power supply to give a voltage of 18V.
5. Assign static IP address at both GBC and Linux PC.
6. Establish communication by pinging each other.
7. Validate the output as per the above requirement.

##### **Reference**

Further details can be found in Page 41, 56 and 57 of GBC schematic Life-2.

### TIVA Ethernet

#### Test Setup



**Figure 46.TIVA Ethernet - Test Setup Diagram**

#### Test Case: Electrical validation (Test ID: ETH.3.1)

##### **Description**

1. **Purpose**The purpose of this test case is to verify MDI electrical characteristics Interface between Marvell Switch (88E6071) and TIVA
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Packet loss and data inconsistency |
| Performance | Yes | Data transfer will be affected |
| Compliance | NA |  |

**Table 352. Impact of Failure of EV – *TIVA Ethernet***

1. **Measurement Locations**

T10.16, T10.14, T10.11 AND T10.9

##### **Test Equipment List**

1. Oscilloscope: DPO7354C
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: DPO7354C

Voltage per division: 500mV

Time scale: 50ns

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. HDMI Monitor

##### **Software Requisites**

1. Ethernet driver
2. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 353. Test Condition for EV – *TIVA Ethernet***

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test | Measuring Point | Measuring Criteria | Specification | |
| Min | Max |
| T\_ETHSW\_TIVA\_P0\_TXP**/** TXN **(**From Port to Switch) | | | | |
| TXP  TXN | T10.16, T10.14 | Vp-p (V) | 1.9 | 2.63 |
| Overshoot (%) | 0 | 10 |
| Undershoot (%) | 0 | 10 |
| T\_TIVA\_ETHSW\_P0\_RXP **/** RXN **(**From Switch to TIVA) | | | | |
| RXP  RXN | T10.11 T10.9 | Vp-p (V) | 1.9 | 2.63 |
| Overshoot (%) | 0 | 10 |
| Undershoot (%) | 0 | 10 |

**Table 354. Requirements for EV – *TIVA Ethernet***

##### **Test Procedure**

1. Connect Debug board to GBC board with OS and Ethernet driver installed
2. Connect a monitor to debug board using HDMI cable
3. Connect a Linux PC to port A of GBC board.
4. Configure DC power supply to give a voltage of 18V.
5. Flash the relevant code to TIVA so that signals between Port 0 of Marvell switch and TIVA are initiated
6. The MDI transmit signals (from Port to Switch) are measured at T10.16 (TXP) and T10.14 (TXN).
7. The MDI receiving signals (from Switch to TIVA) are measured at T10.11 (RXP) and T10.9 (RXN).
8. Make sure the measuring criteria for the signal satisfies the above mentioned requirements.

##### **Reference**

Further details can be found in Page 56 and 59 of GBC schematic Life-2.

#### Test Case: Functional Validation (Test ID: ETH.3.2)

##### **Description**

1. **Purpose**The purpose of the test case is to validate the function of TIVA – Marvel switch MDI transfer.
2. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | Registers of SOC become inaccessible on failure of this test case and data transfer can be affected. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 355. Impact of Failure of FV – *TIVA Ethernet***

##### **Test Equipment List**

1. Oscilloscope: DPO7354C
2. DC power supply: E3633A

##### **Equipment Settings**

1. Oscilloscope: DPO7354C

Voltage per division: 500mV

Time scale: 50ns

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 19V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Debug board
3. HDMI Monitor

##### **Software Requisites**

1. Ethernet driver
2. OS loaded MSATA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 356. Test Condition of FV – *TIVA Ethernet***

##### **DUT Settings**

NA.

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Test** | **Measuring Parameter** | **Result** |
| Ethernet Interface | Data transfer | Flash the relevant code to TIVA so that signals between Port 0 of Marvell switch and TIVA are initiated. Once IP address is assigned to TIVA, initiate the communication by pinging from PC using the “TCPSendRecieve “executable file |

**Table 357. Requirements for FV – *TIVA Ethernet***

##### **Test Procedure**

1. Connect Debug board to GBC board with OS and Ethernet driver installed
2. Connect a monitor to debug board using HDMI cable
3. Connect a Linux PC to port A of GBC board.
4. Configure DC power supply to give a voltage of 18V.
5. Assign IP address.
6. Establish communication by pinging each other.
7. Validate the output as per the above requirement.

##### **Reference**

Further details can be found in Page 56 and 59 of GBC schematic Life-2.

# Clock

## Test Purpose and Description

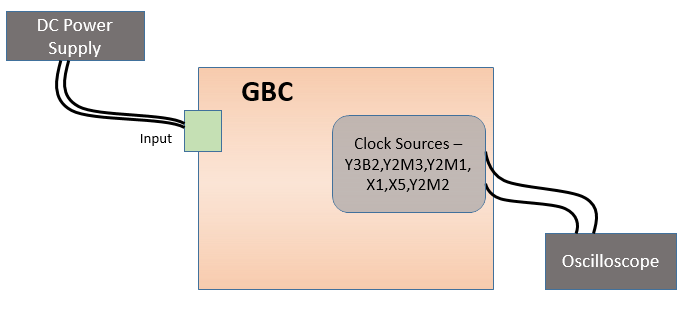
The purpose is to measure the frequency accuracy, jitter and signal integrity of different clocks available in the system.

## Clock Sub-system constitutes of below components

1. Clock sources
2. PCIe - GBE clock
3. 40MHz Ref clock
4. HDMI clock
5. GPS 1pps clock

### Clock Sources

#### Test Setup



**Figure 47. Clock Sources - Test Setup Diagram**

#### Test Case: Frequency Accuracy (Test ID: CLK.1.1)

##### **Description**

1. **Purpose**

The purpose of this test case is to validate the frequency accuracy of crystal sources for 25MHz and 32.768 kHz.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | If clock source is improper, it affects the internal software functionality. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 358. Impact of failure - Clock Sources – Frequency Accuracy**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| Y3B2 | C3B22.1 |
| Y2M3 | C2M26.2 |
| Y2M1 | C2M2.2 |
| X1 | C475.1 |
| X5 | C521.1 |
| Y2M2 | C2N1.2 |

**Table 359. Measurement Locations – Clock Sources – Frequency Accuracy**

##### **Test Equipment List**

1. AUX Power supply unit: Agilent E3634A
2. Oscilloscope: DSA91304A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 20V

OCP: 2A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal Input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 360. Test Condition – Clock Sources – Frequency Accuracy**

##### **DUT Settings**

1. Isolate input side of Tiva controller by removing the resistor R10054.
2. Isolate input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **Measurement location** | **Range** |
| 25MHz crystal frequency | C3B22.1, C2M26.2, C2M2.2, C475.1, C521.1 | 25MHz |
| 32.768kHz RTC crystal frequency | C2N1.2 | 32.768kHz |

**Table 361. Requirements – Clock Sources – Frequency Accuracy**

##### **Test Procedure**

1. This test is conducted for the following 25MHz crystals:
   * 1. Y3B2 at C3B22.1
     2. Y2M3 at C2M26.2
     3. Y2M1 at C2M2.2
     4. X1 at C475.1
     5. X5 at C521.1
2. This test is also conducted for the following 32.768kHz crystal:
   * 1. Y2M2 at C2N1.2
3. The values are captured by a frequency counter. For frequency accuracy and stability measured value (Hz) is converted to ppb by following the below procedure:
4. The difference between the ideal clock frequency and maximum frequency value is calculated (df).
5. Ppb is calculated by the equation: ppb= (df (Hz)\*〖10〗^6\*1000) / (f (Hz))

##### **Reference**

Further details can be found in Page 9, 23, 25, 56 and 58 of GBC schematic Ver. Life-2.

#### Test Case: Timing Jitter (Test ID: CLK.1.2)

##### **Description**

1. **Purpose**

The purpose of this test case is to validate the timing jitter of crystal clock sources.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | If clock source is improper, it affects the internal software functionality. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 362. Impact of failure - Clock Sources – Frequency Accuracy**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| Y3B2 | C3B22.1 |
| Y2M3 | C2M26.2 |
| Y2M1 | C2M2.2 |
| X1 | C475.1 |
| X5 | C521.1 |

**Table 363. Measurement Locations – Clock Sources – Timing Jitter**

##### **Test Equipment List**

1. AUX Power supply unit: Agilent E3634A
2. Oscilloscope: DSA91304A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 20V

OCP: 2A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal Input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 364. Test Condition – Clock Sources – Timing Jitter**

##### **DUT Settings**

1. Isolate input side of Tiva controller by removing the resistor R10054.
2. Isolate input side of Intel microprocessor by removing the resistor R10067.

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **Measurement location** | **Range (ps)** |
| Cycle-to-cycle Jitter(ps) | Y3B2 | 0 – 300 |
| X5 | 0 – 50 |
| X1 | 0 – 300 |

**Table 365. Requirements – Clock Sources – Timing Jitter**

##### **Test Procedure**

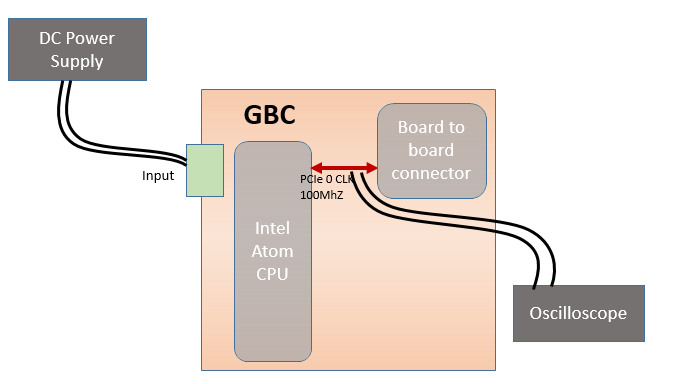
1. This test is conducted for the following 25MHz crystals:
   1. Y3B2 at C3B22.1.
   2. Y2M3 at C2M26.2.
   3. Y2M1 at C2M2.2.
   4. X1 at C475.1.
   5. X5 at C521.1
2. The jitter values are captured by an oscilloscope.

##### **Reference**

Further details can be found in Page 9, 23, 25, 56 and 58 of GBC schematic Ver. Life-2.

### PCIe - GBE clock

#### Test Setup



**Figure 48. PCIe – GBE Clock - Test Setup Diagram**

#### Test Case: Frequency Accuracy (Test ID: CLK.2.1)

##### **Description**

1. **Purpose**

Purpose of this test case is to validate the frequency accuracy of 100MHz PCIe reference clock: PCIE0\_GBE\_CLKP.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | If clock source is improper, it affects the internal software functionality. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 366. Impact of failure - PCIe – GBE Clock – Frequency Accuracy**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| PCIE0\_GBE\_CLKP | R10647.1 |

**Table 367. Measurement Locations – PCIe – GBE Clock – Frequency Accuracy**

##### **Test Equipment List**

1. AUX Power supply unit: Agilent E3634A
2. Oscilloscope: DSA91304A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 20V

OCP: 2A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal Input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 368. Test Condition – PCIe – GBE Clock – Frequency Accuracy**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **Measurement location** | **Range** |
| PCIE0\_GBE\_CLKP | R10647.1 | 100MHz |

**Table 369. Requirements – PCIe – GBE Clock – Frequency Accuracy**

##### **Test Procedure**

1. This test is conducted by probing 100MHz clock at R10647.1.
2. The value is captured by a frequency counter for 6 iterations.
3. For frequency accuracy and stability measured value (Hz) is converted to ppb by following the below procedure:
4. The difference between the ideal clock frequency and maximum frequency value is calculated (df).
5. Ppb is calculated by the equation:

##### **Reference**

Further details can be found in Page 9 and 76 of GBC schematic Ver. Life-2.

#### Test Case: Signal Integrity (Test ID: CLK.2.2)

##### **Description**

1. **Purpose**

Purpose of the test case is to validate the electrical characteristics of 100 MHz PCIe clock

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | If clock source is improper, it affects the PCIe communication and functionality. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 370. Impact of failure - PCIe – GBE Clock – Signal Integrity**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| PCIE0\_GBE\_CLKP | R10647.1 |

**Table 371. Measurement Locations – PCIe – GBE Clock – Signal Integrity**

##### **Test Equipment List**

1. AUX Power supply unit: Agilent E3634A
2. Oscilloscope: DSA91304A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 20V

OCP: 2A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal Input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 372. Test Condition – PCIe – GBE Clock – Signal Integrity**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **Measurement location** | **Range (V)** |
| Positive Over-shoot | R10647.1 | 0 – 0.18 |
| Negative Over-shoot | R10648.1 | 0 – 0.18 |

**Table 373. Requirements – PCIe – GBE Clock – Signal Integrity**

##### **Test Procedure**

1. This test is conducted by probing 100MHz clock at R10647.1.
2. The value is captured on an oscilloscope and is within the prescribed limit by Intel microcontroller.

##### **Reference**

Further details can be found in Page 9and 76 of GBC schematic Ver. Life-2.

#### Test Case: Timing Jitter (Test ID: CLK.2.3)

##### **Description**

1. **Purpose**

Purpose of the test case is to validate the Timing Jitter of 100 MHz

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | If clock source is improper, it affects the PCIe communication and functionality. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 374. Impact of failure - PCIe – GBE Clock – Timing Jitter**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| PCIE0\_GBE\_CLKP | R10647.1 |
| PCIE0\_GBE\_CLKN | R10648.1 |

**Table 375. Measurement Locations – PCIe – GBE Clock – Timing Jitter**

##### **Test Equipment List**

1. AUX Power supply unit: Agilent E3634A
2. Oscilloscope: DSA91304A

##### **Test Equipment List**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 20V

OCP: 2A

##### **Hardware Requisites**

1. GBC board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal Input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 376. Test Condition – PCIe – GBE Clock – Timing Jitter**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **Measurement location** | **Range** |
| PCIE0\_GBE\_CLKP  PCIE0\_GBE\_CLKN | R10647.1  R10648.1 | 100MHz |

**Table 377. Requirements – PCIe – GBE Clock – Timing Jitter**

##### **Test Procedure**

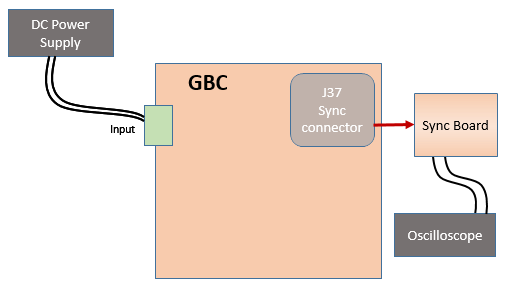
1. This test is conducted by terminating PCIE0\_GBE\_CLKP and with a 2.2pF capacitor at R10647.1 and R10648.1.
2. Probe at R10647.1 and R10648.1. Run the test utility N5393D in the infiniium oscilloscope.
3. To configure the test suite, select PCIe version as 2.0, Refclk tests, Device1, Lan0. In select tests option in utility, select common clock tests and run all the selected test cases.
4. The test utility generates the test report for all the test cases selected with the pass or fail criteria and its % margin.

##### **Reference**

Further details can be found in Page 9and 76 of GBC schematic Ver. Life-2.

### 40 MHz - GPSDO clock

#### Test Setup



**Figure 49. 40 MHz GPSDO– Clock - Test Setup Diagram**

#### Test Case: Frequency Accuracy (Test ID: CLK.3.1)

##### **Description**

1. **Purpose**

Purpose of this test case is to validate the frequency accuracy of 40MHz reference clock for GPSDO.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | If clock source is improper, it affects the GPS sync frequency and sync time functionality. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 378. Impact of failure – 40 MHz GPSDO– Clock – Frequency Accuracy**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| R\_LTE\_REF\_OUT\_10MHz | R19.2 |

**Table 379. Measurement Locations – 40 MHz GPSDO– Clock – Frequency Accuracy**

##### **Test Equipment List**

1. AUX Power supply unit: Agilent E3634A
2. Oscilloscope: DSA91304A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 20V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Sync board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal Input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 380. Test Condition – 40 MHz GPSDO– Clock – Frequency Accuracy**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **Measurement location** | **Range** |
| R\_LTE\_REF\_OUT\_10MHz | R19.2 | 40MHz |

**Table 381. Requirements – 40 MHz GPSDO– Clock – Frequency Accuracy**

##### **Test Procedure**

1. This test is conducted by probing 40MHz clock at R19.2.
2. The value is captured by a frequency counter.

##### **Reference**

Further details can be found in Page 3 of Sync Schematic Ver. Life-1.

#### Test Case: Signal Integrity (Test ID: CLK.3.2)

##### **Description**

1. **Purpose**

Purpose of the test case is to validate the electrical characteristics of 40 MHz GPSDO clock.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | If clock source is improper, it affects the GPS sync frequency and sync time functionality. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 382. Impact of failure – 40 MHz GPSDO– Clock – Signal Integrity**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| R\_LTE\_REF\_OUT\_10MHz | R19.2 |

**Table 383. Measurement Locations – 40 MHz GPSDO– Clock – Signal Integrity**

##### **Test Equipment List**

1. AUX Power supply unit: Agilent E3634A
2. Oscilloscope: DSA91304A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 20V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Sync board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal Input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 384. Test Condition – 40 MHz GPSDO– Clock – Signal Integrity**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **Measurement location** | **Range (V)** |
| R19.2 | VLOW | 0 – 0.4 |
| VHIGH | 0.8 – 3.3 |

**Table 385. Requirements – 40 MHz GPSDO– Clock – Signal Integrity**

##### **Test Procedure**

1. This test is conducted by probing the GPSDO Clock signal at R19.2 (Near Via).
2. The measured values must be well with-in the limit as specified in the LTE-Lite Module datasheet specification.

##### **Reference**

Further details can be found in Page 3 of Sync Schematic Ver. Life-1.

#### Test Case: Timing Jitter (Test ID: CLK.3.3)

##### **Description**

1. **Purpose**

The purpose of the test case is to validate the Timing Jitter of 40 MHz GPSDO Clock.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | If clock source is improper, it affects the GPS sync frequency and sync time functionality. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 386. Impact of failure – 40 MHz GPSDO– Clock – Timing Jitter**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| R\_LTE\_REF\_OUT\_10MHz | R19.2 |

**Table 387. Measurement Locations – 40 MHz GPSDO– Clock – Timing Jitter**

##### **Test Equipment List**

1. AUX Power supply unit: Agilent E3634A
2. Oscilloscope: DSA91304A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 20V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Sync board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal Input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 388. Test Condition – 40 MHz GPSDO– Clock – Timing Jitter**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **Measurement location** | **Range** |
| R\_LTE\_REF\_OUT\_10MHz | R19.2 | 40MHz |

**Table 389. Requirements – 40 MHz GPSDO– Clock – Timing Jitter**

##### **Test Procedure**

1. This test is conducted by probing the GPSDO Clock Signal Timing Jitter at R19.2 (Near Via). The measurement data will be compared with the measured data that will be made available by Jacksons Lab.
2. Steps to measure RMS jitter through signal analyzer:
   1. Connect Sync board to GBC board.
   2. Configure DC power supply to give a voltage of 18V.
   3. Set the central frequency to 40MHz in MXA signal Analyzer.
   4. Carrier frequency will be automatically detected.
   5. Go to Mode option, Select Phase Noise.
   6. Go to Measure option and select Log Plot.
   7. In Span option set start and stop offset values to 8kHz and 22MHz respectively
   8. Select marker go to Integrated RMS Noise then select Jitter option.
   9. Go to Band adjust set the left band (10 KHz) and right band (22MHz).
   10. Measure the Jitter on the analyzer in pico second.
   11. Select auto tune in frequency option at the end of each step.

##### **Reference**

Further details can be found in Page 3 of Sync Schematic Ver. Life-1.

### HDMI clock

#### Test Setup



**Figure 50. HDMI– Clock - Test Setup Diagram**

#### Test Case: Frequency Accuracy (Test ID: CLK.4.1)

##### **Description**

1. **Purpose**

Purpose of this test case is to validate the frequency accuracy of HDMI clock.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | If clock source is improper, it affects the HDMI communication between Intel and external HDMI device |
| Performance | NA |  |
| Compliance | NA |  |

**Table 390. Impact of failure – HDMI Clock – Frequency Accuracy**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| HDMI\_CLK\_DP | C4N2.2 |
| HDMI\_CLK\_DN | C4N1.2 |

**Table 391. Measurement Locations – HDMI Clock – Frequency Accuracy**

##### **Test Equipment List**

1. AUX Power supply unit: Agilent E3634A
2. Oscilloscope: DSA91304A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 20V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Sync board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal Input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 392. Test Condition – HDMI Clock – Frequency Accuracy**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **Measurement location** | **Range** |
| HDMI\_CLK\_DP | C4N2.2 | 100MHz |
| HDMI\_CLK\_DN | C4N1.2 |

**Table 393. Requirements – HDMI Clock – Frequency Accuracy**

##### **Test Procedure**

1. This test is conducted by probing 40MHz clock at R19.2.
2. The value is captured by a frequency counter.

##### **Reference**

Further details can be found in Page 7 and 69 of GBC schematic Ver. Life-2 and also on page 2 of Debug Schematic Ver. Life-2.

#### Test Case: Signal Integrity (Test ID: CLK.4.2)

##### **Description**

1. **Purpose**

The purpose of the test case is to validate the electrical characteristics of 100 MHz HDMI Clock.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | If clock source is improper, it affects the HDMI communication between Intel and external HDMI device |
| Performance | NA |  |
| Compliance | NA |  |

**Table 394. Impact of failure – HDMI Clock – Signal Integrity**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| HDMI\_CLK\_DP | C4N2.2 |
| HDMI\_CLK\_DN | C4N1.2 |

**Table 395. Measurement Locations – HDMI Clock – Signal Integrity**

##### **Test Equipment List**

1. AUX Power supply unit: Agilent E3634A
2. Oscilloscope: DSA91304A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 20V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Sync board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal Input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 396. Test Condition – HDMI Clock – Signal Integrity**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **Measurement location** | **Range (V)** |
| Positive Over-shoot | C4N2.2 &  C4N1.2 | 0 – 0.78 |
| Negative Over-shoot | 0 – 0.2 |

**Table 397. Requirements – HDMI Clock – Signal Integrity**

##### **Test Procedure**

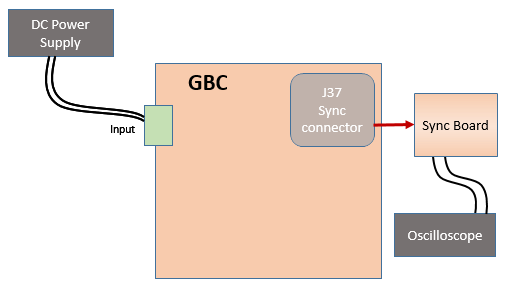
1. Connect debug board to GBC. Probe HDMI\_CLK\_DP and HDMI\_CLK\_DN at C4N2.2 and C4N1.2 respectively.
2. Measure the overshoot and undershoot parameters for HDMI clock using oscilloscope.

##### **Reference**

Further details can be found in Page 7 and 69 of GBC schematic Ver. Life-2 and also on page 2 of Debug Schematic Ver. Life-2.

### GPS – 1pps clock

#### Test Setup



**Figure 51. GPS 1pps Clock - Test Setup Diagram**

#### Test Case: Frequency Accuracy (Test ID: CLK.5.1)

##### **Description**

1. **Purpose**

The purpose of this test case is to validate the 1pps clock.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | If clock source is improper, it affects the GPS sync frequency and sync time functionality. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 398. Impact of failure – GPS 1pps Clock – Frequency Accuracy**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| R\_LTE\_1\_PPS\_OUT | R48.1 |

**Table 399. Measurement Locations – GPS 1pps Clock – Frequency Accuracy**

##### **Test Equipment List**

1. AUX Power supply unit: Agilent E3634A
2. Oscilloscope: DSA91304A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 20V

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Sync board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal Input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 400. Test Condition – GPS 1pps Clock – Frequency Accuracy**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **Measurement location** | **Range** |
| R\_LTE\_1\_PPS\_OUT | R48.1 | 1Hz |

**Table 401. Requirements – GPS 1pps Clock – Frequency Accuracy**

##### **Test Procedure**

1. Connect Sync board to GBC board. Probe R48.1 on sync board in order to check 1pps clock.
2. Measure the frequency using frequency counter.

##### **Reference**

Further details can be found in Page 3 of Sync Schematic Ver. Life-1.

#### Test Case: Signal Integrity (Test ID: CLK.5.2)

##### **Description**

1. **Purpose**

The purpose of the test case is to validate the electrical characteristics of 1pps clock.

1. **Impact of failure of test case on system**

|  |  |  |
| --- | --- | --- |
| **Impact** | **Applicable** | **Description** |
| Functional | Yes | If clock source is improper, it affects the GPS sync frequency and sync time functionality. |
| Performance | NA |  |
| Compliance | NA |  |

**Table 402. Impact of failure – GPS 1pps Clock – Signal Integrity**

1. **Measurement Locations**

|  |  |
| --- | --- |
| **Measurement Parameter** | **Measurement location** |
| R\_LTE\_1\_PPS\_OUT | R48.1 |

**Table 403. Measurement Locations – GPS 1pps Clock – Signal Integrity**

##### **Test Equipment List**

1. AUX Power supply unit: Agilent E3634A
2. Oscilloscope: DSA91304A

##### **Equipment Settings**

1. DC power supply: E3633A

Supply Voltage: 18V

Current Limit: 1.5A

OVP: 20V

OCP: 2A

OCP: 2A

##### **Hardware Requisites**

1. GBC board
2. Sync board

##### **Software Requisites**

NA

##### **Test Condition**

|  |  |  |
| --- | --- | --- |
| **Test condition** | **Value** | **Remarks** |
| Voltage | 18V | Nominal Input voltage |
| Temperature | +25 C | Normal Room temperature |

**Table 404. Test Condition – GPS 1pps Clock – Signal Integrity**

##### **DUT Settings**

NA

##### **Requirements**

|  |  |  |
| --- | --- | --- |
| **Measurement Parameter** | **Measurement location** | **Range** |
| R\_LTE\_1\_PPS\_OUT | R48.1 | 1Hz |

**Table 405. Requirements – GPS 1pps Clock – Signal Integrity**

##### **Test Procedure**

1. Connect Sync board to GBC board. This test is conducted by probing 1pps clock at R48.1 on the sync board.
2. The value is captured on an oscilloscope.

##### **Reference**

Further details can be found in Page 3 of Sync Schematic Ver. Life-1.