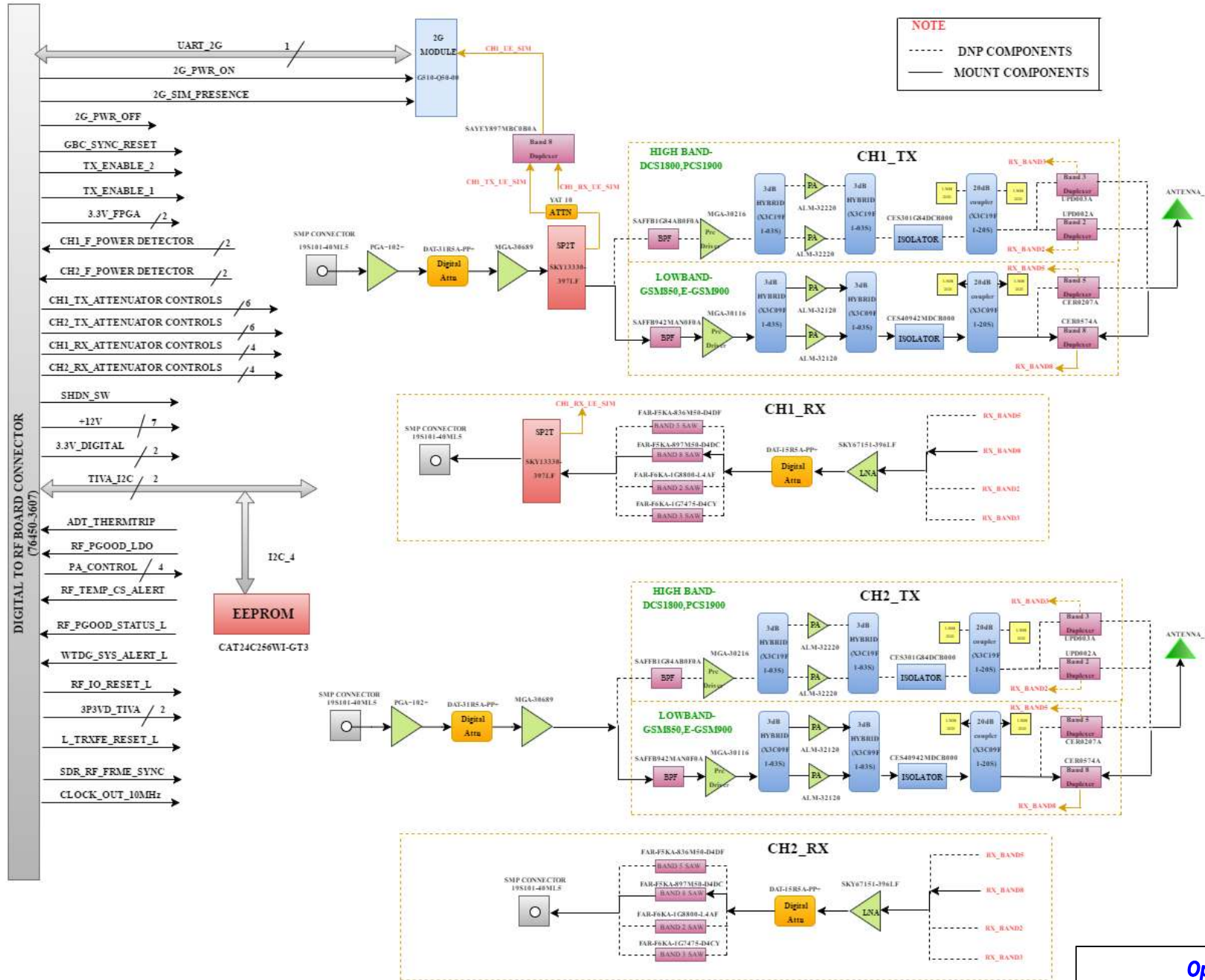


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37	PA ENABLES
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41	TEMPARATURE SENSOR

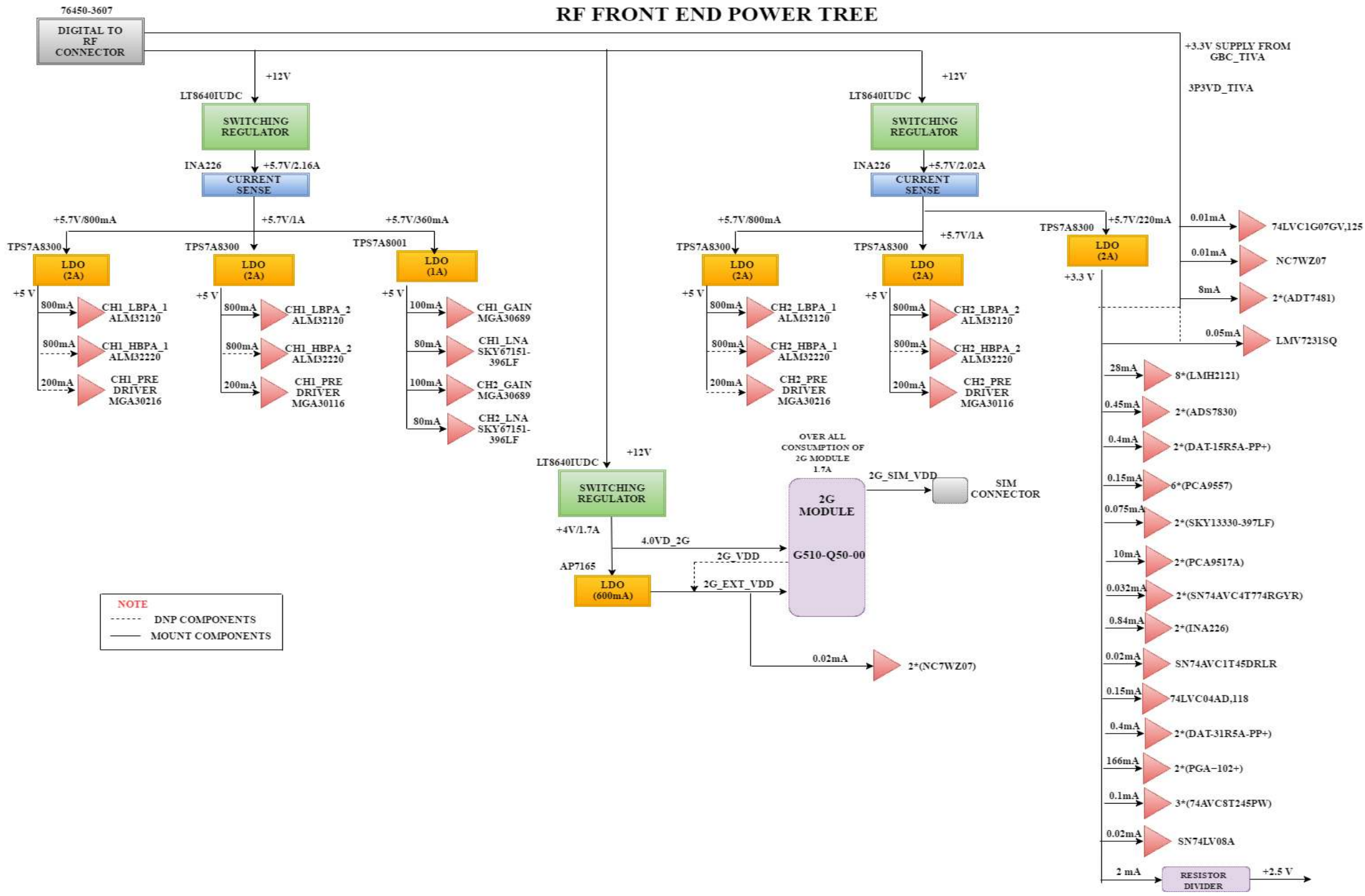
REVISION HISTORY			
DATE	VERSION	UPDATED BY	REMARKS
02 FEB 2016	1.00		REV A RELEASE
16 JUN 2016	2.00		REV B RELEASE
30 NOV 2016	3.00		REV C RELEASE

RF FRONT END BLOCK DIAGRAM

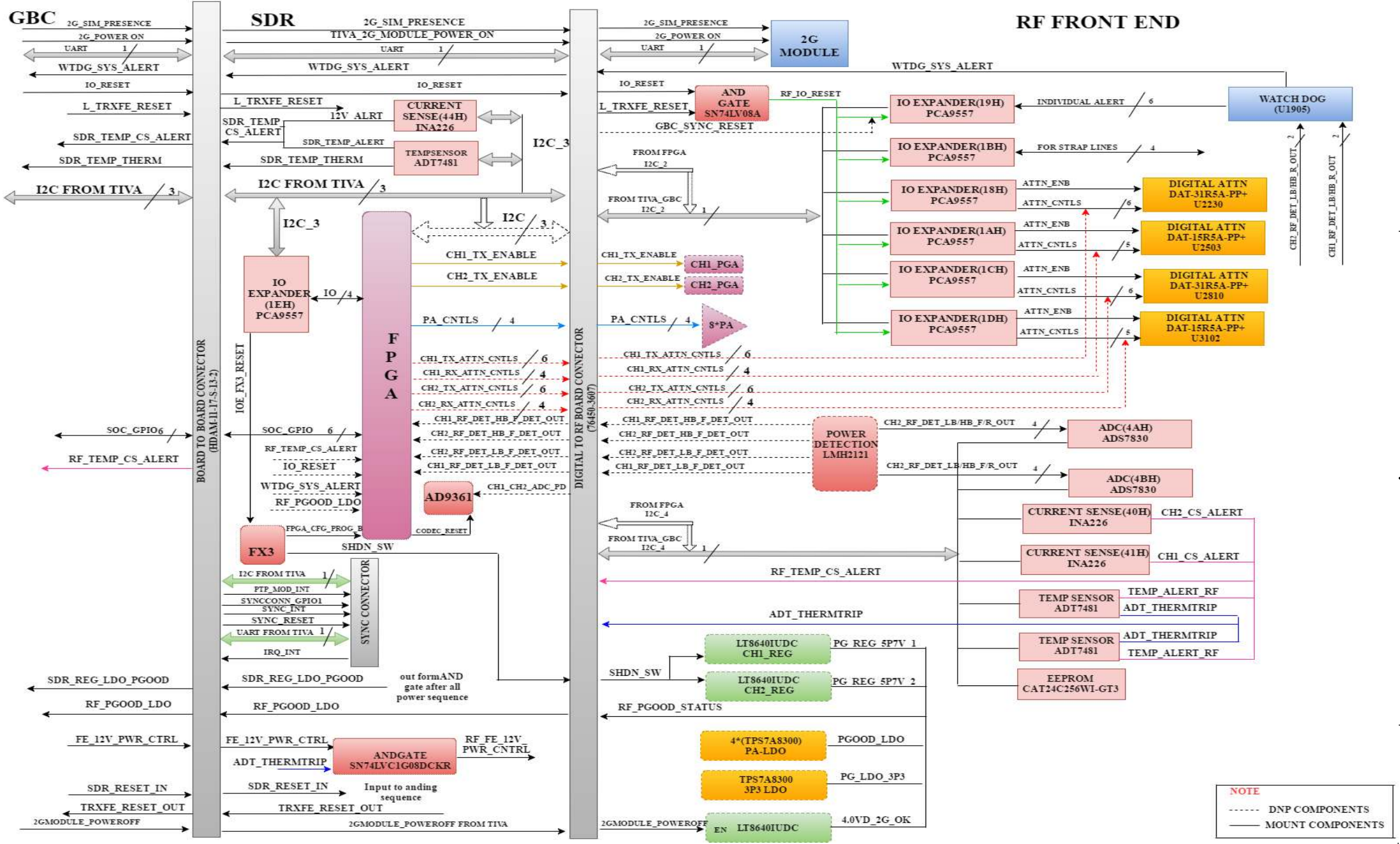


OpenCellular connect-1		
Title RF Block Diagram		
Size A3	Document Number 00	Rev 1.0
Date: Thursday, December 01, 2016 Sheet 2 of 41		

RF FRONT END POWER TREE



OpenCellular connect-1		
POWER TREE		
Title		
Size	Document Number	Rev
A3	FBCON1RFSOCSC001	1.0
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REG_12V_5P7V

Place the testpoint TP57 near to the power plane P12V

LT8640_INT_VCC_1 internal 3.4V regulator Bypass (Do not load the INTVCC pin with external circuitry)

Place the testpoint TP58 near to the power plane 5P7V_REG_1

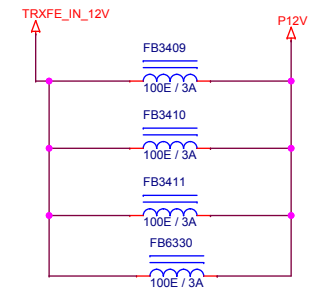
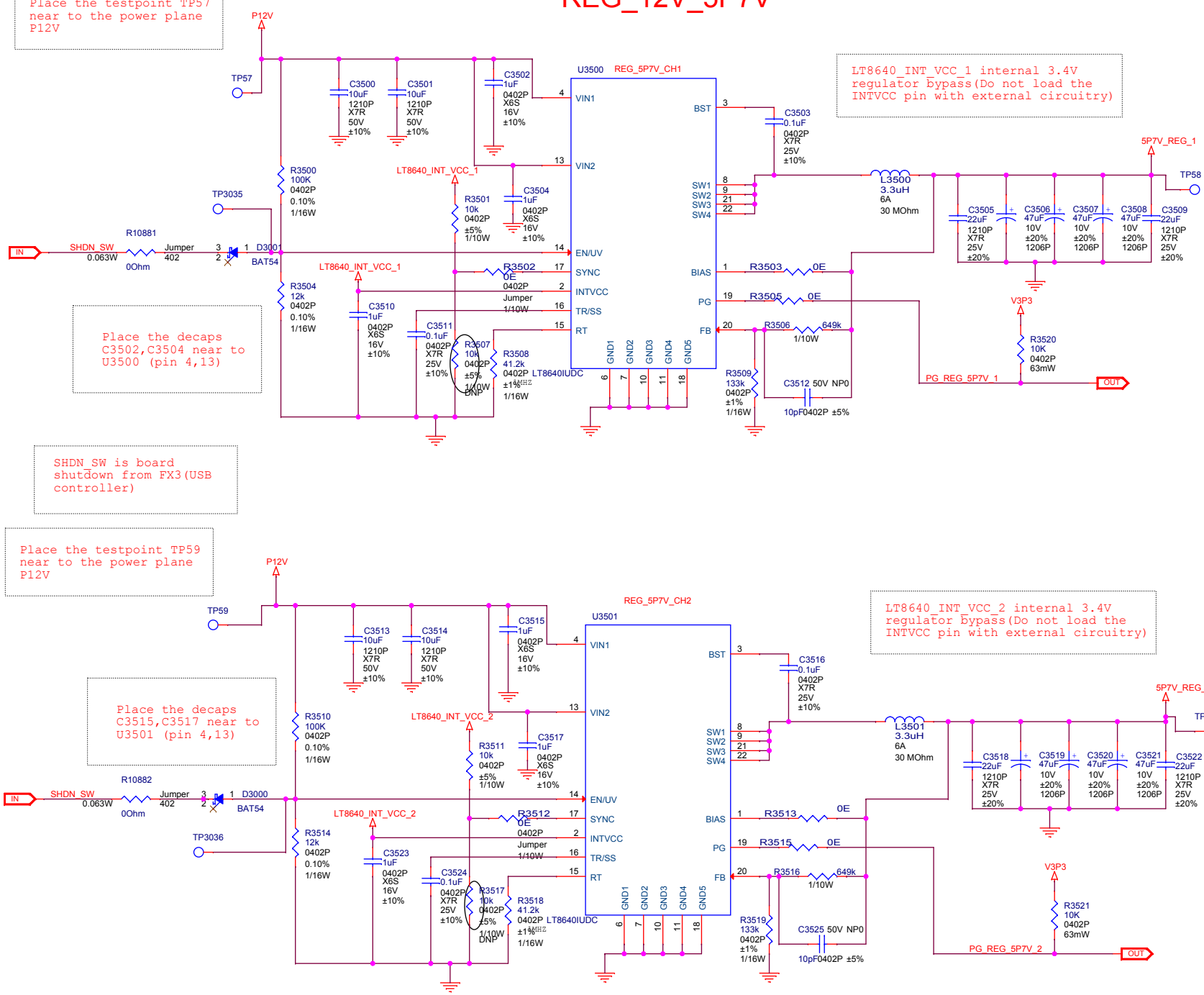
Place the decaps C3502, C3504 near to U3500 (pin 4,13)

SHDN SW is board shutdown from FX3 (USB controller)

Place the testpoint TP59 near to the power plane P12V

Place the decaps C3515, C3517 near to U3501 (pin 4,13)

Place the testpoint TP60 near to the power plane 5P7V_REG_2



OpenCellular connect-1		
Title	REG_12V_5P7V	
Size	Document Number	Rev
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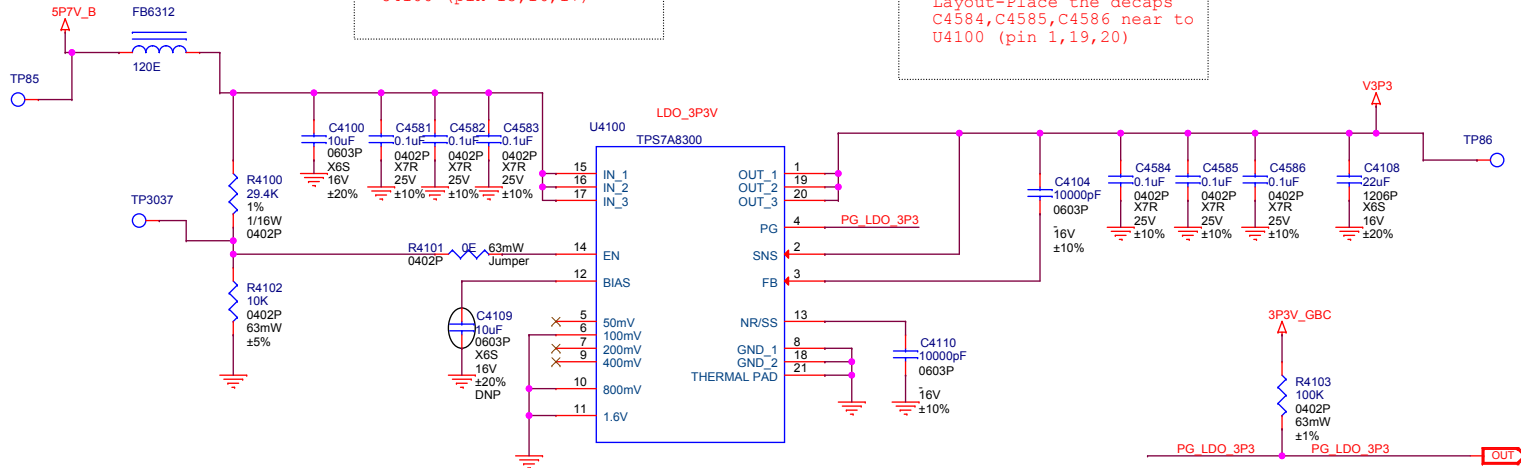
LDO_3P3V_LDO_5V

Layout-Place the testpoint TP85 near to the power plane 5P7V_B

Layout-Place the decaps C4581,C4582,C4583 near to U4100 (pin 15,16,17)

Layout-Place the decaps C4584,C4585,C4586 near to U4100 (pin 1,19,20)

Place the testpoint TP86 near to the power plane V3P3

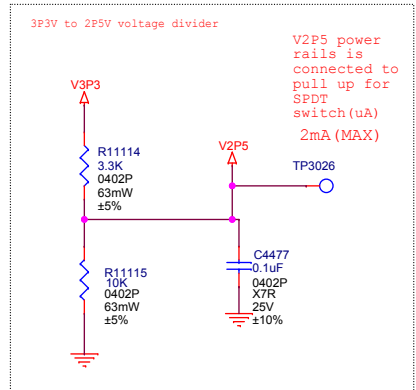
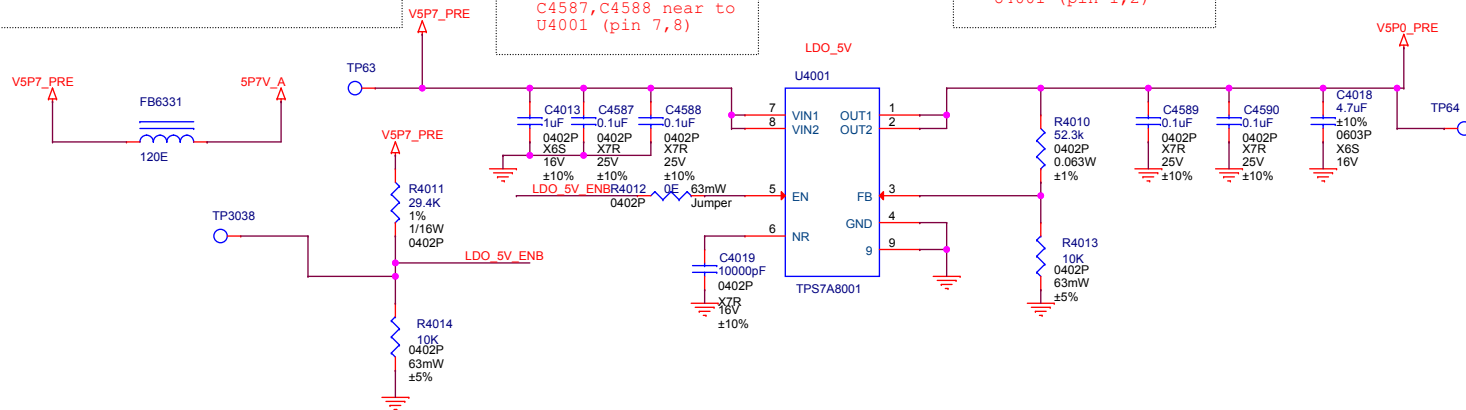


Layout-Place the testpoint TP63 near to the power plane V5P7_PRE

Place the decaps C4587,C4588 near to U4001 (pin 7,8)

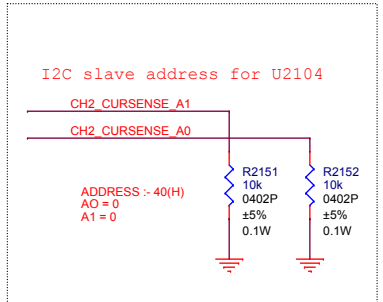
Place the decaps C4589,C4590 near to U4001 (pin 1,2)

Place the testpoint TP64 near to the power plane V5P0_PRE

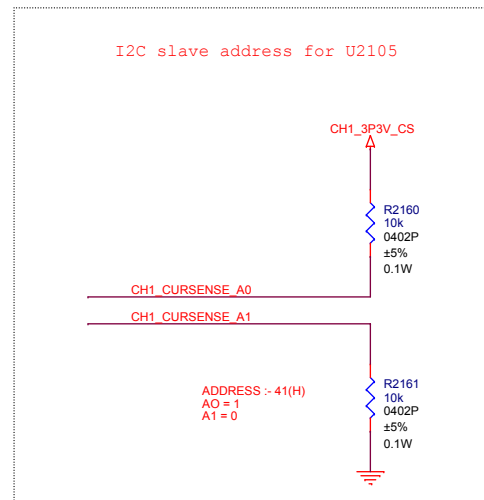
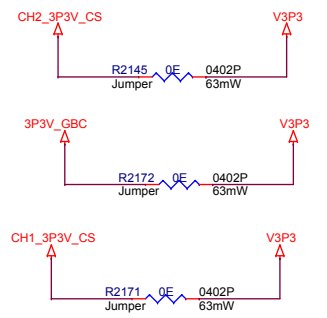
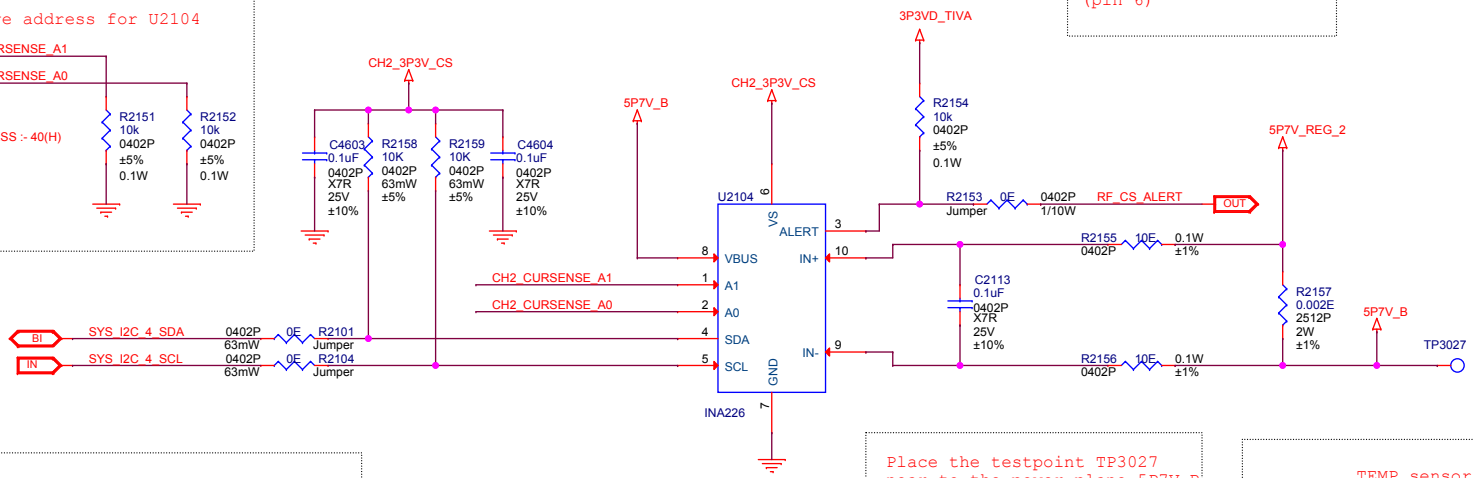


OpenCellular connect-1		
Title		
REG_3P3V_LDO_5V		
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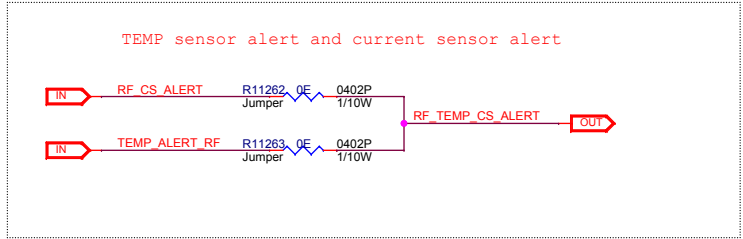
CURRENT SENSING FOR CH1&CH2



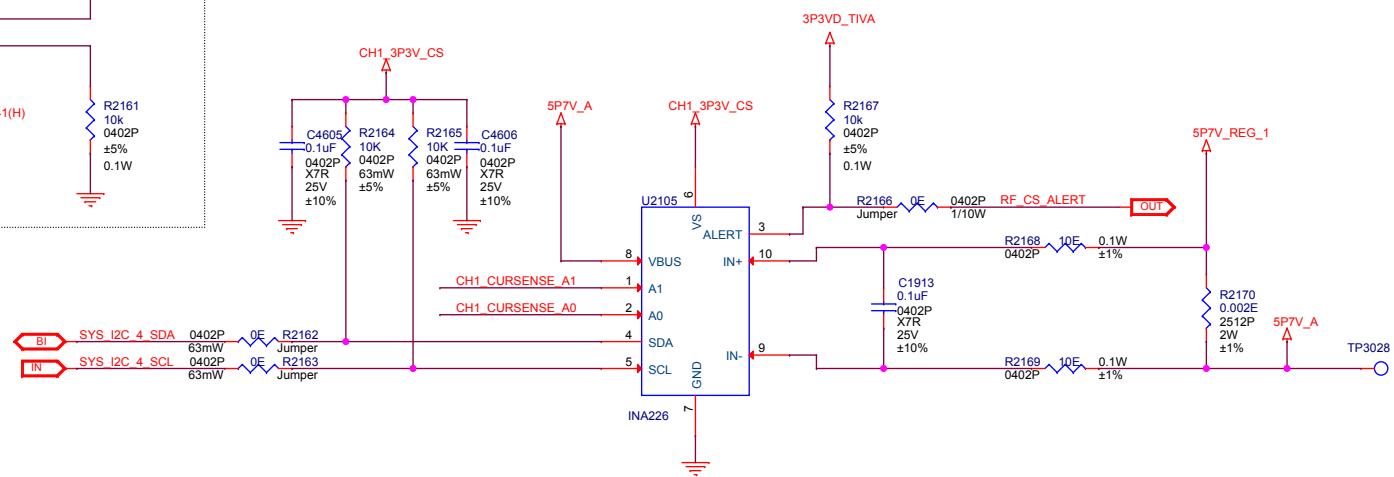
Layout-Place the decap C4604 near to U2104 (pin 6)



Place the testpoint TP3027 near to the power plane 5P7V_B



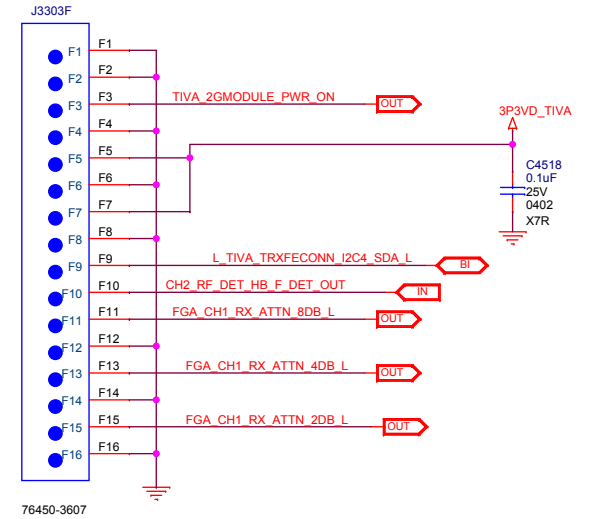
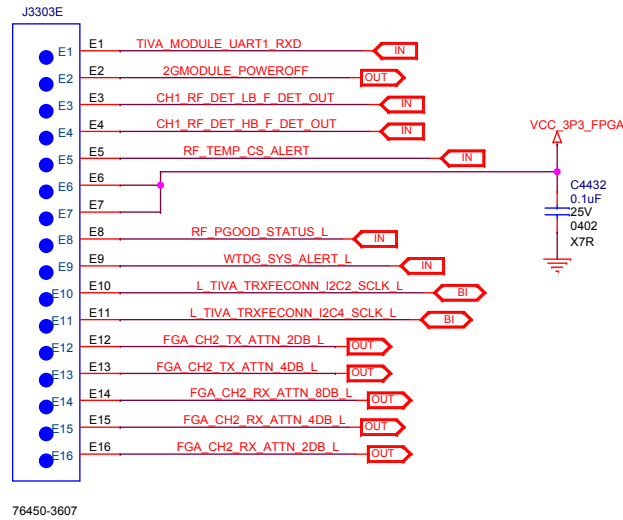
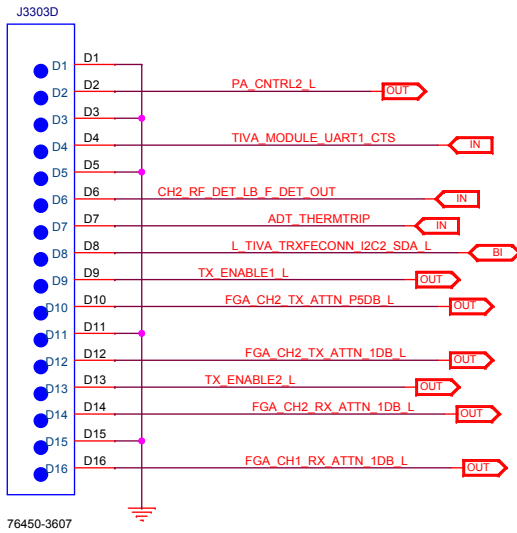
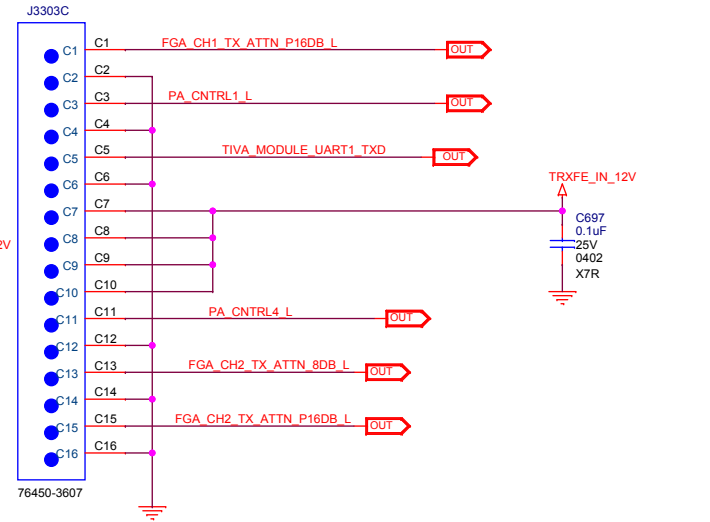
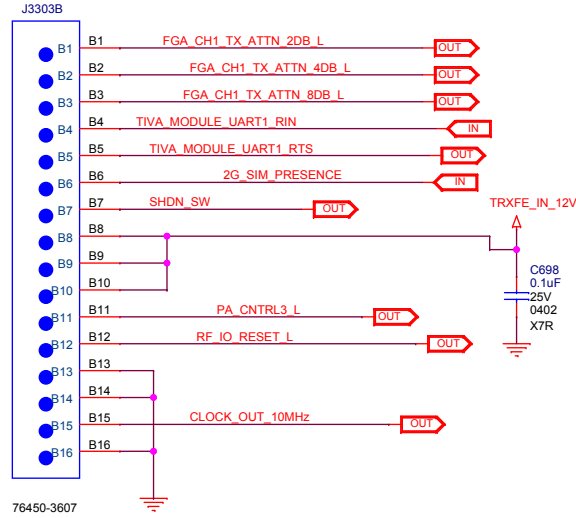
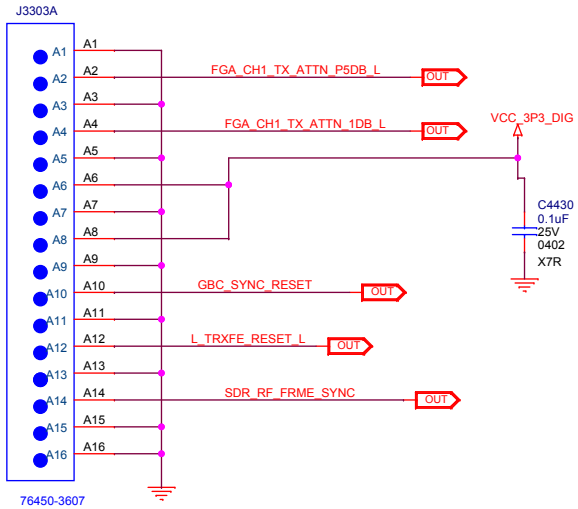
Layout-Place the decaps C4606 near to U2105 (pin 6)



Place the testpoint TP3028 near to the power plane 5P7V_A

OpenCellular connect-1		
Title		
CUR SENSE FOR CH1&CH2		
Size A3	Document Number 00	Rev 1.0
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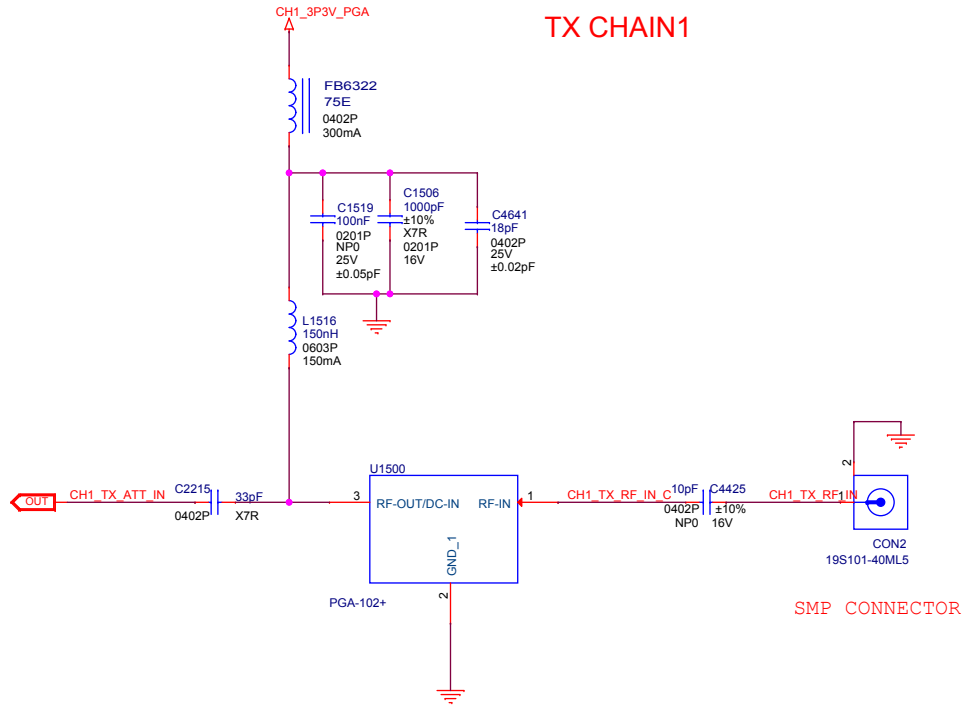
DIGITAL BOARD CONNECTOR



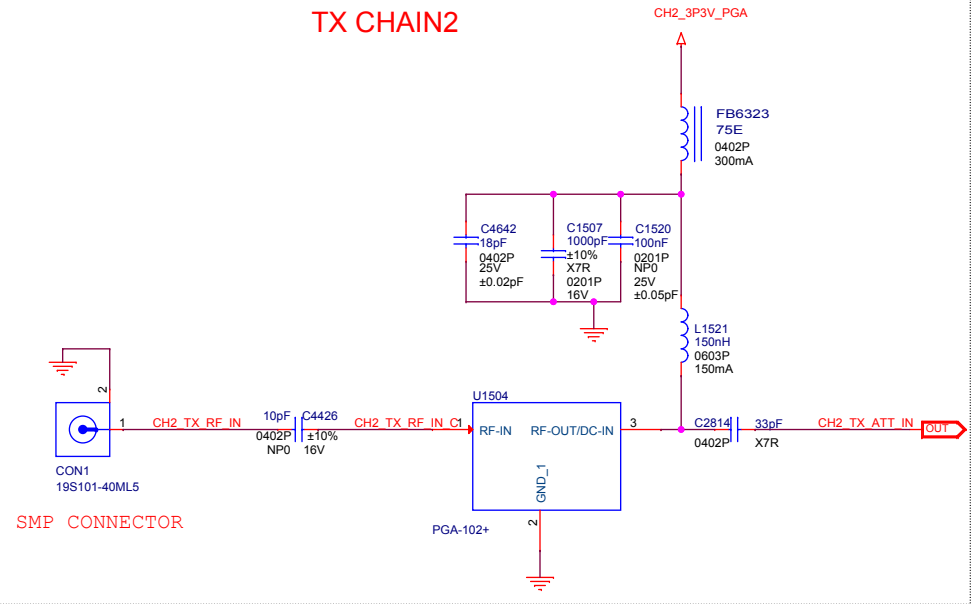
OpenCellular connect-1		
Title: DIG CONNECTOR		
Size: A3	Document Number: FBCON1RFSOCSCH001	Rev: 1.0
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TX_RF_CONNECTOR

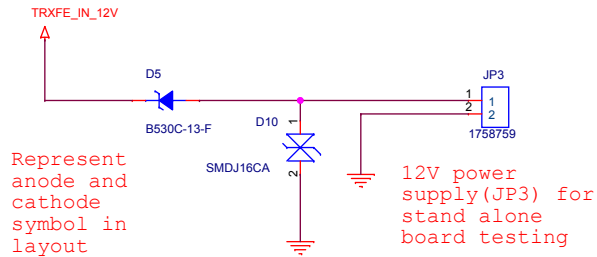
TX CHAIN1



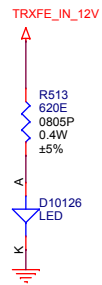
TX CHAIN2



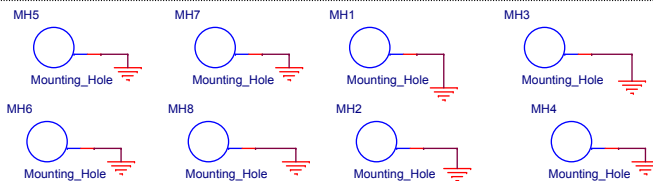
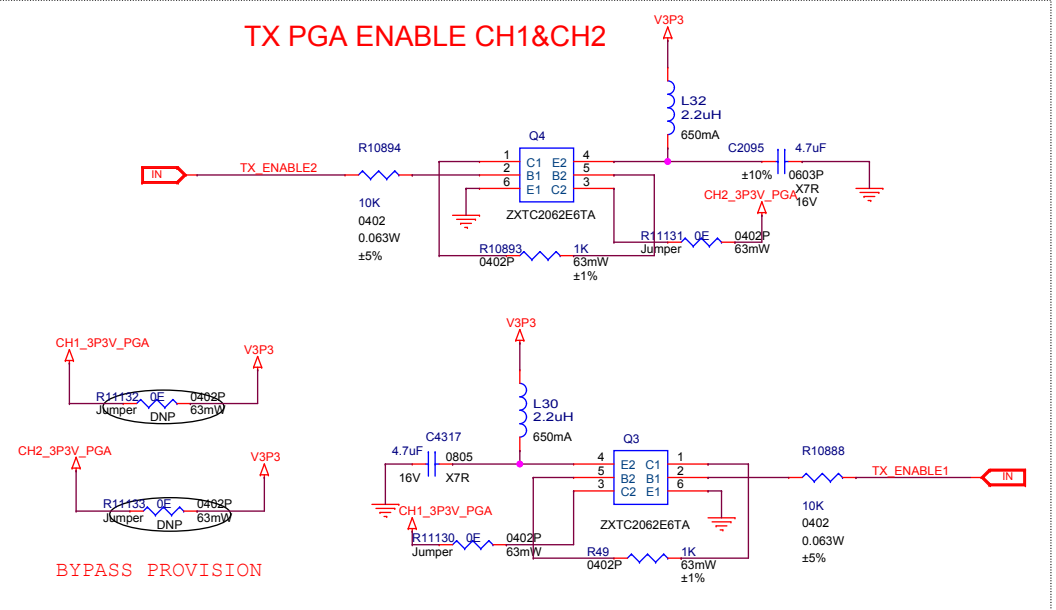
12 Volt Supply



12 Volt LED



TX PGA ENABLE CH1&CH2

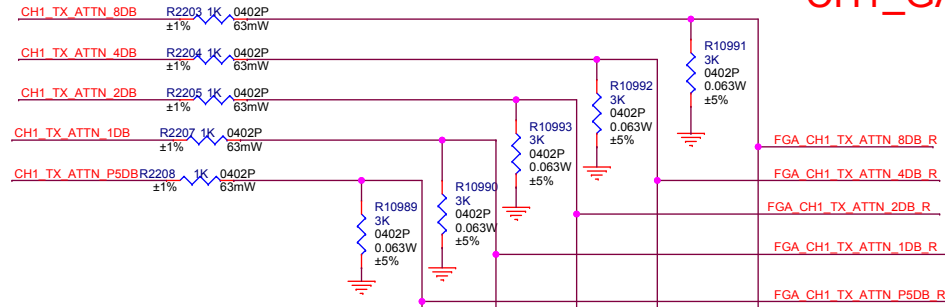


MOUNTING HOLES

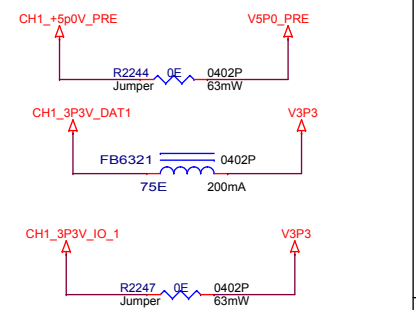
OpenCellular connect-1

Title			TX_RF_CONNECTOR		
Size	Document Number	Rev			
A3	FBCON1RF5OCSCSH001	1.0			
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CH1_GAIN_ATT



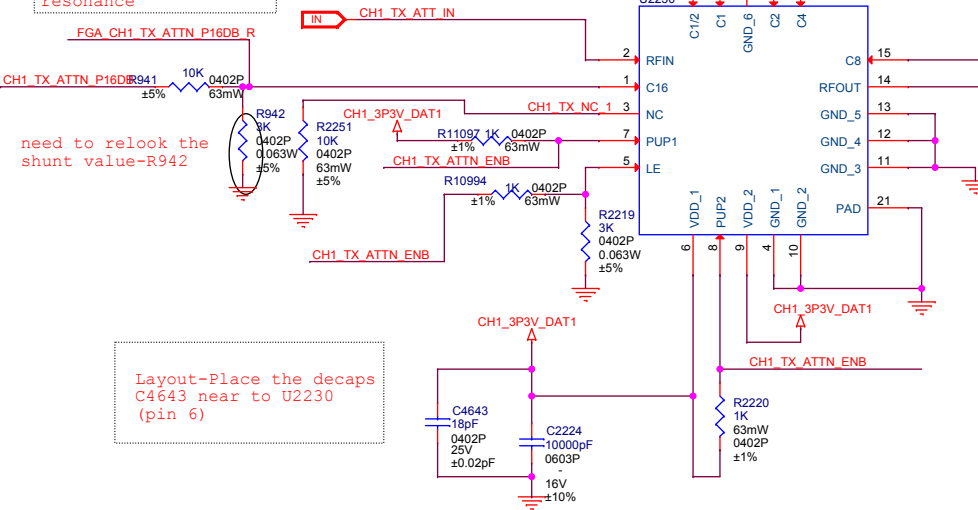
C4519, C2240, C2241, C2242, L2214, C4520 are the matching for 0.2 to 3 GHz-U2203



Place R941 resistor near to pin 1 on U2230 to avoid freq. resonance

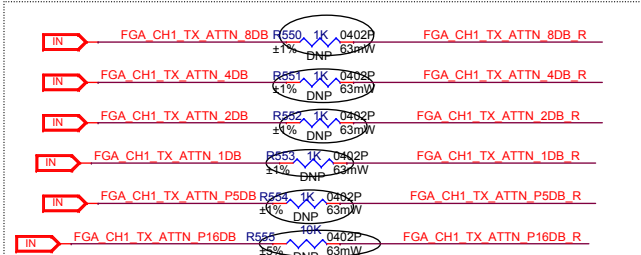
need to relook the shunt value-R942

C4665, C4666 are provision in shunt (DNP) for filtering purpose in future-U2203

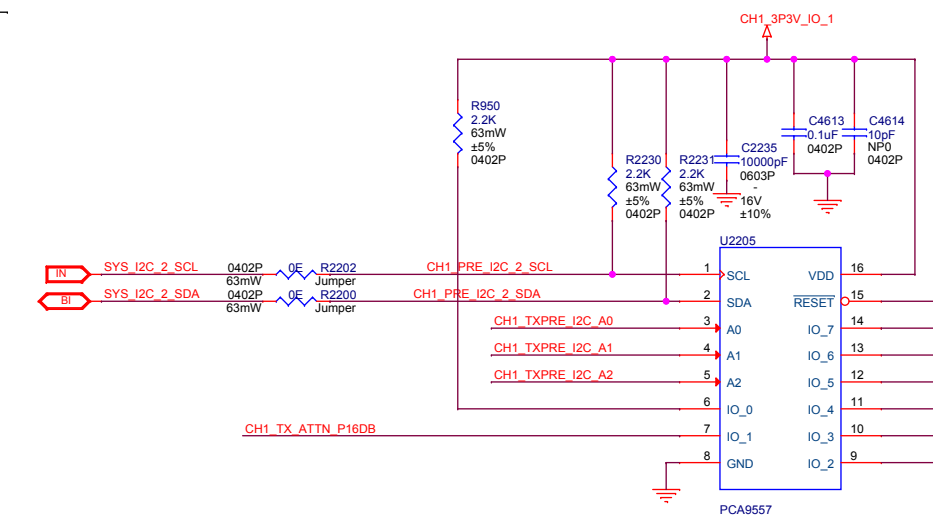


Layout-Place the decaps C4643 near to U2230 (pin 6)

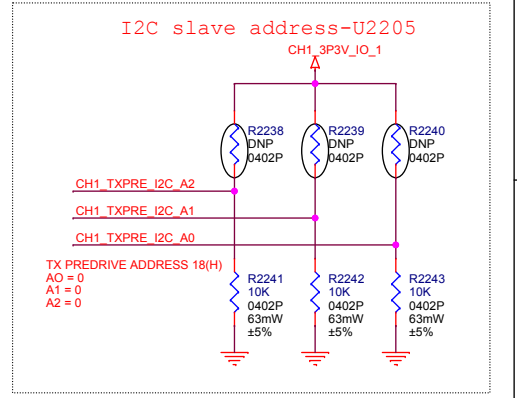
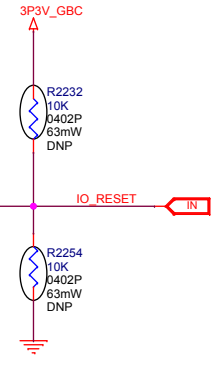
place capacitors C4519, C4520 and C2241 near to pin1, pin 3 of U2203



- 1) When mounted control signals are connected to FPGA
- 2) Layout-Place these resistors close to actual path in order to avoid stubs-Provide crowfoot option



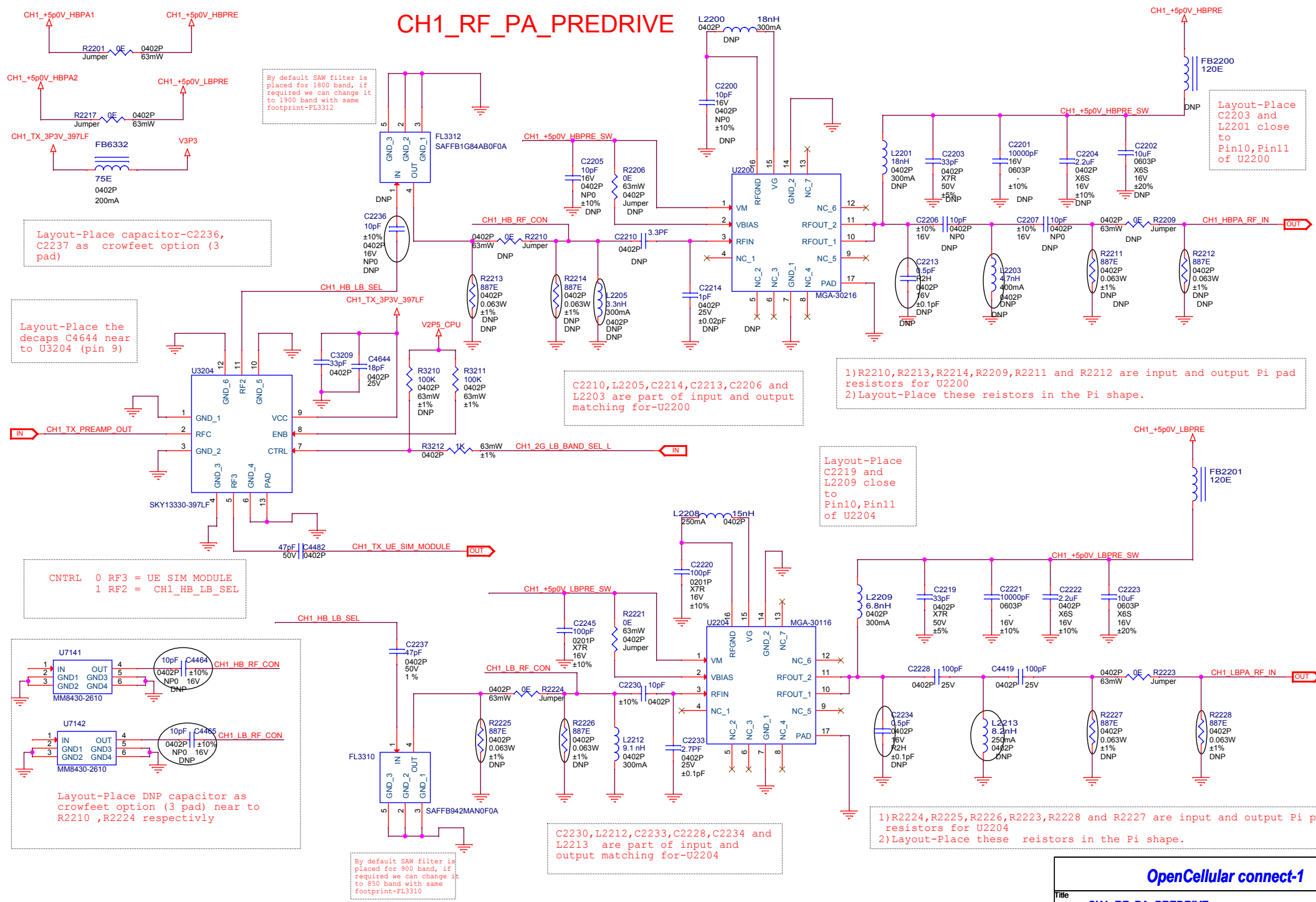
Layout-Place the decaps C4614 near to U2205 (pin 16)



OpenCellular connect-1

Title CH1_GAIN_ATT		
Size A3	Document Number 00	Rev 1.0
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CH1_RF_PA_PREDRIVE



Layout-Place capacitor-C2236, C2237 as crowfeet option (3 pad)

Layout-Place the decaps C4644 near to U3204 (pin 9)

By default SAW filter is placed for 1800 band, if required we can change it to 1900 band with same footprint-FL3312

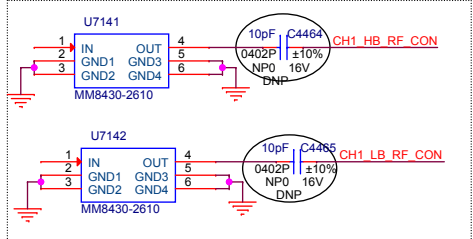
C2210, L2205, C2214, C2213, C2206 and L2203 are part of input and output matching for-U2200

1) R2210, R2213, R2214, R2209, R2211 and R2212 are input and output Pi pad resistors for U2200
2) Layout-Place these resistors in the Pi shape.

Layout-Place C2203 and L2201 close to Pin10, Pin11 of U2200

Layout-Place C2219 and L2209 close to Pin10, Pin11 of U2204

CTRL 0 RF3 = UE SIM MODULE
1 RF2 = CH1_HB_LB_SEL



Layout-Place DNP capacitor as crowfeet option (3 pad) near to R2210, R2224 respectively

By default SAW filter is placed for 900 band, if required we can change it to 850 band with same footprint-FL3310

C2230, L2212, C2233, C2228, C2234 and L2213 are part of input and output matching for-U2204

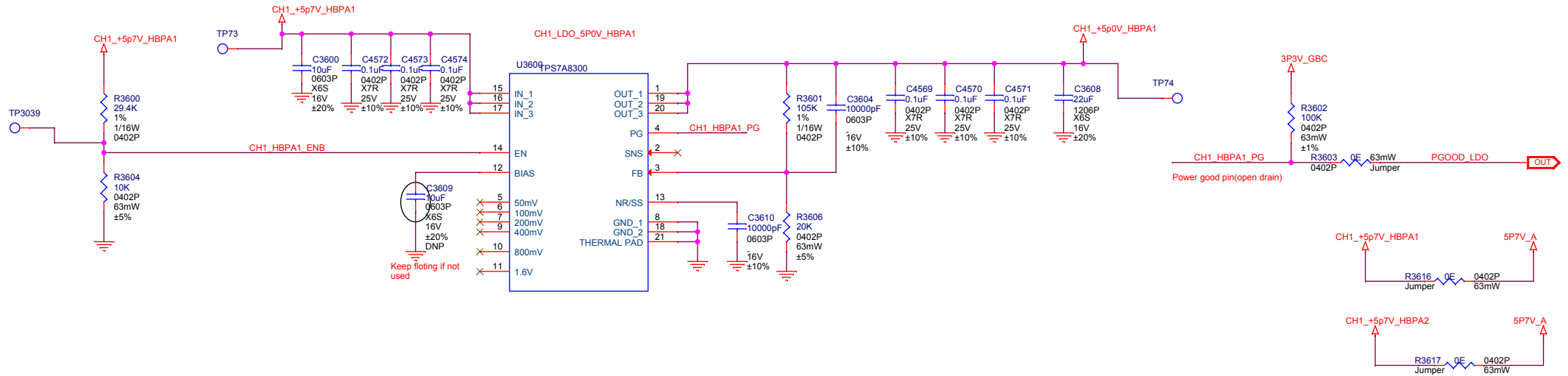
1) R2224, R2225, R2226, R2223, R2228 and R2227 are input and output Pi pad resistors for U2204
2) Layout-Place these resistors in the Pi shape.

OpenCellular connect-1		
Title	CH1_RF_PA_PREDRIVE	
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A3	00	1.0
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CH1_HB_LDO

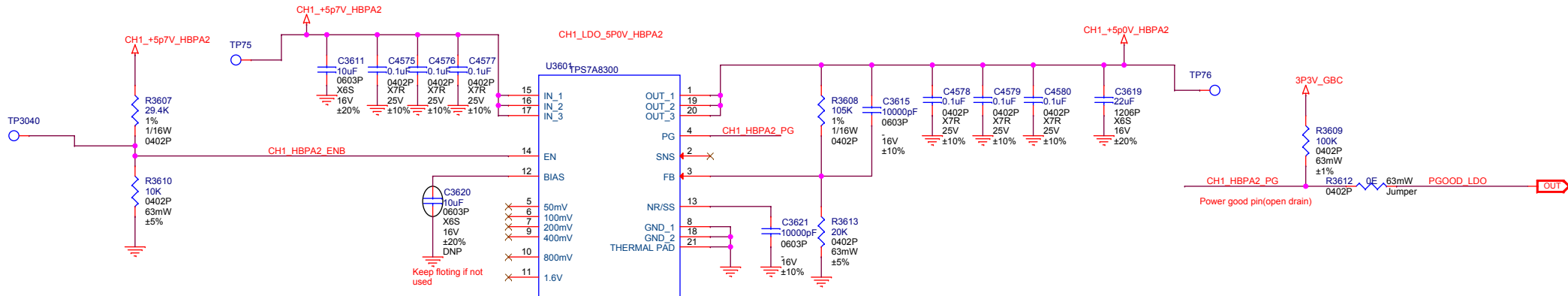
Place the testpoint TP73 near to the power plane CH1_+5p7V_HBPA1-U3600

Place the testpoint TP74 near to the power plane CH1_+5p0V_HBPA1-U3600

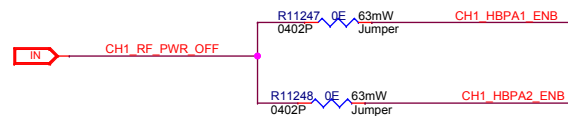


Place the testpoint TP75 near to the power plane CH1_+5p7V_HBPA2-U3601

Place the testpoint TP76 near to the power plane CH1_+5p0V_HBPA2-U3601



CH1 power off control



OpenCellular connect-1

Title		
CH1_HB_LDO		
Size	Document Number	Rev
A3	00	1.0
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CH1_RF_PA_LB

Layout-Place DNP capacitor-C4413 as crowfeet option (3 pad) near to C4447

Layout-1)Place C2403 capacitor near to pin 20 of -U2400
2)Place C2404 capacitor near to pin 18 of U2400

C2410,C2413,L2402,C2411,C2414,C4421 and L2403 are part of input and output matching for-U2400

R11159,R11158,R11160 are the 2dB PI pad resistors for the input port of-U2400

R853,R854,R855 are the PI pad resistors for the ISO port of-U2403

R850,R851,R852 are the PI pad resistors for the ISO port of-U2402

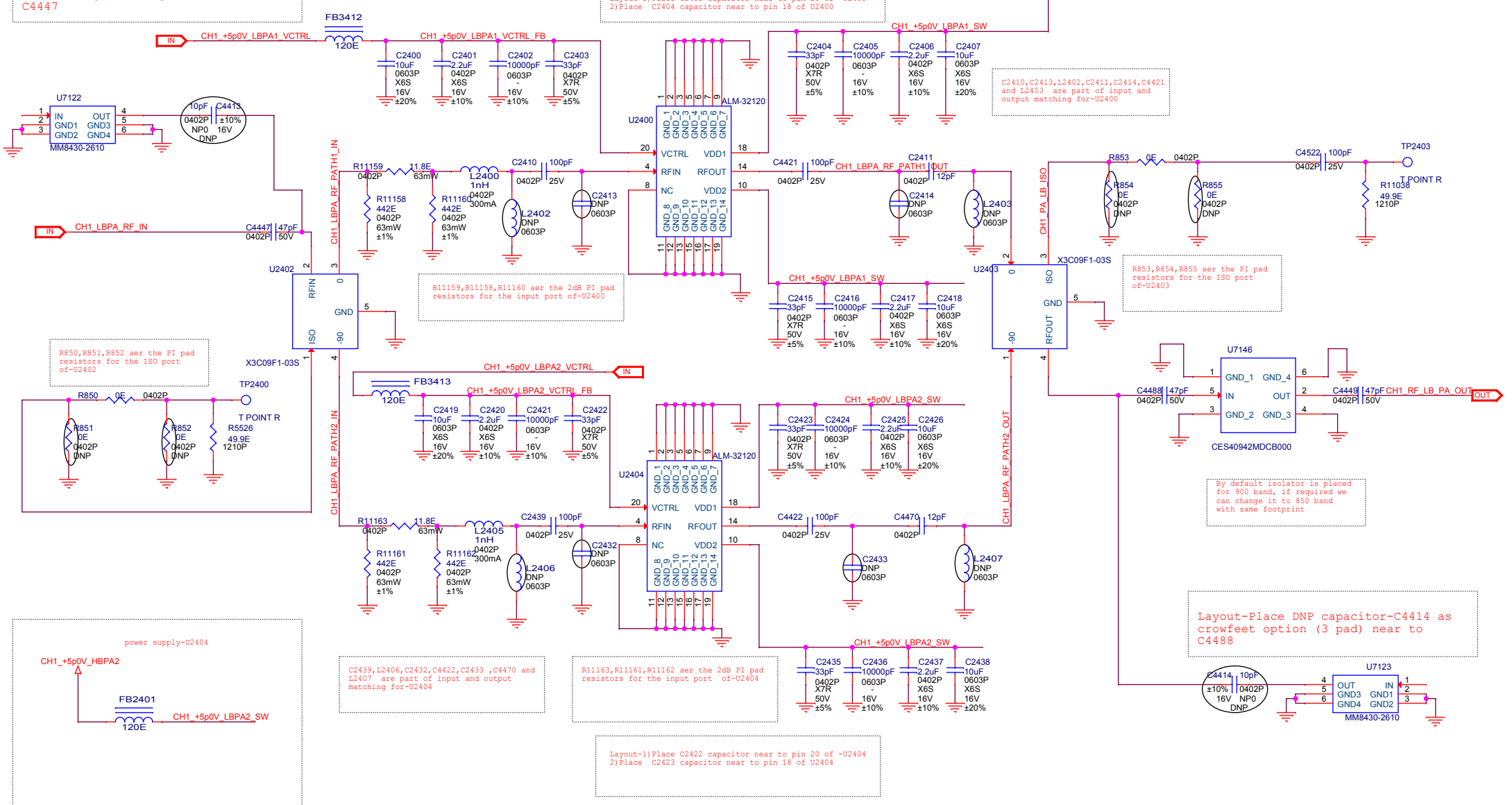
By default inductor is placed for 900 band, if required we can change it to 850 band with same footprint

Layout-Place DNP capacitor-C4414 as crowfeet option (3 pad) near to C4488

C2439,L2406,C2432,C4422,C2433 ,C4470 and L2407 are part of input and output matching for-U2404

R11163,R11161,R11162 are the 2dB PI pad resistors for the input port of-U2404

Layout-1)Place C2422 capacitor near to pin 20 of -U2404
2)Place C2423 capacitor near to pin 18 of U2404



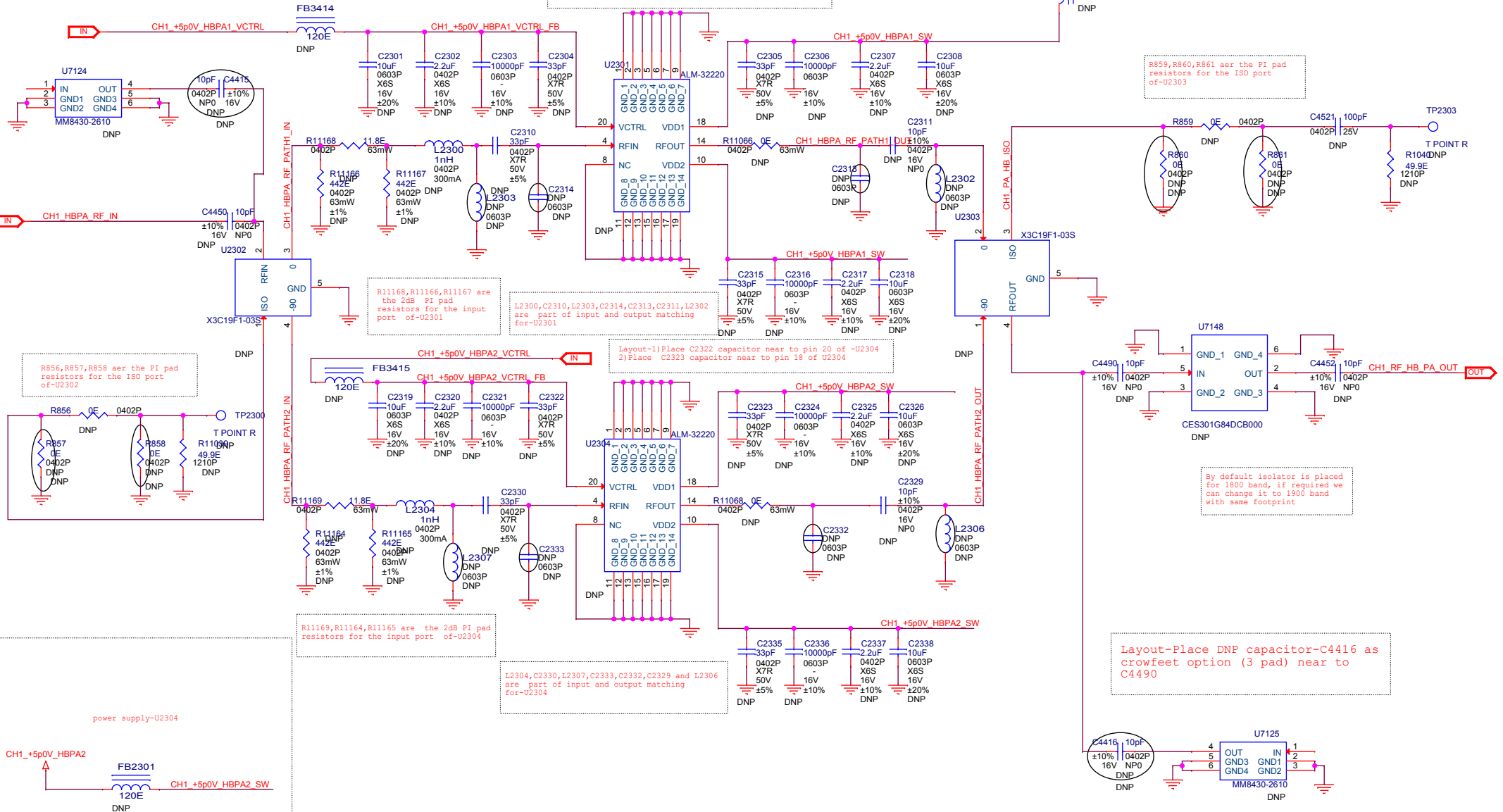
OpenCellular connect-1		
Title CH1_RF_PA_LB		
Size A3	Document Number 00	Rev 1.0
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CH1_RF_PA_HB

Layout-Place DNP capacitor-C4415 as crowfeet option (3 pad) near to C4450

Layout-1)Place C2304 capacitor near to pin 20 of -U2301
2)Place C2305 capacitor near to pin 18 of U2301

R859,R860,R861 are the PI pad resistors for the ISO port of-U2303



R11169,R11166,R11167 are the 2dB PI pad resistors for the input port of-U2301

L2300,C2310,L2303,C2314,C2313,C2311,L2302 are part of input and output matching for-U2301

Layout-1)Place C2322 capacitor near to pin 20 of -U2304
2)Place C2323 capacitor near to pin 18 of U2304

By default isolator is placed for 1800 band, if required we can change it to 1900 band with same footprint

R11169,R11164,R11165 are the 2dB PI pad resistors for the input port of-U2304

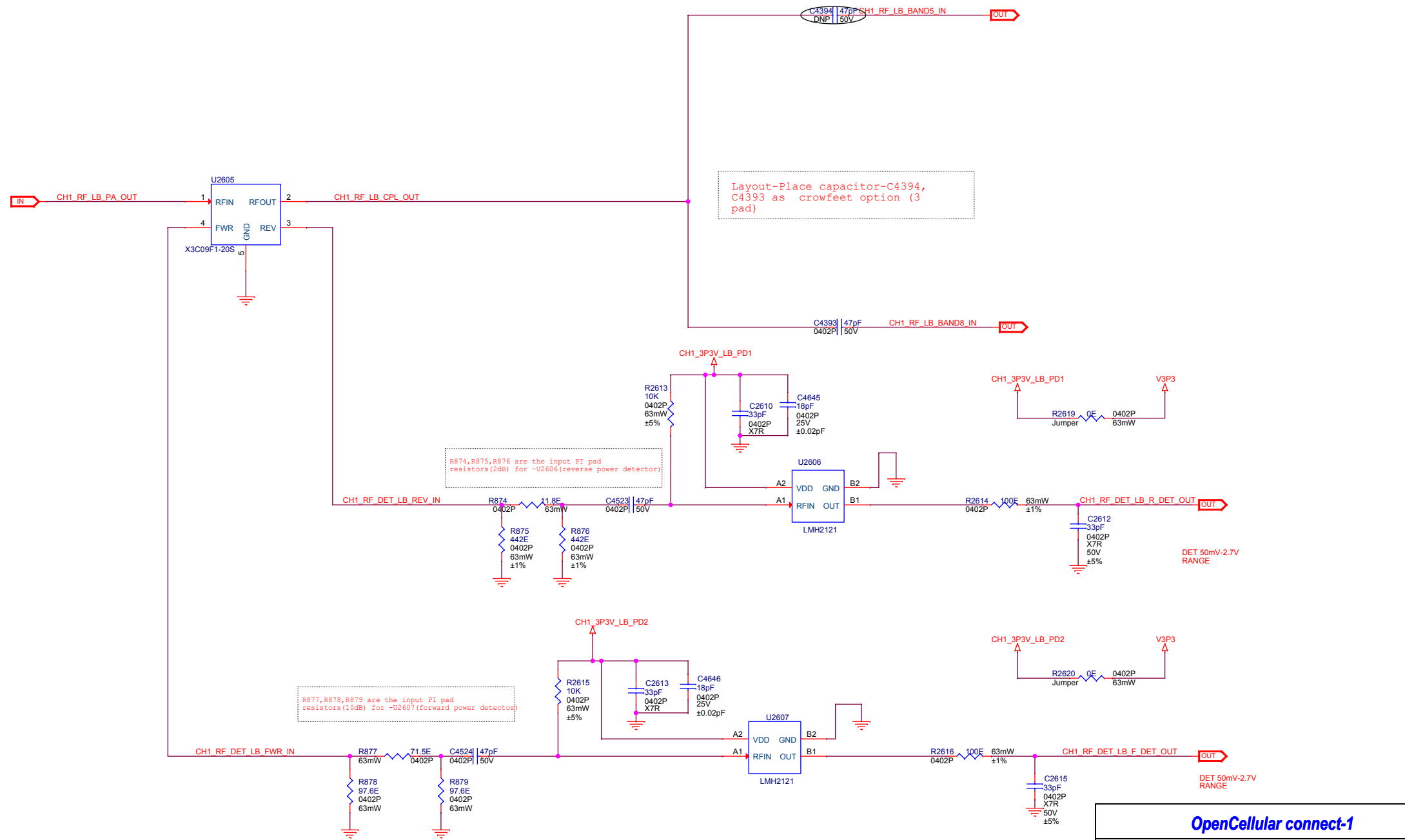
L2304,C2330,L2307,C2333,C2332,C2329 and L2306 are part of input and output matching for-U2304

Layout-Place DNP capacitor-C4416 as crowfeet option (3 pad) near to C4490

power supply-U2304

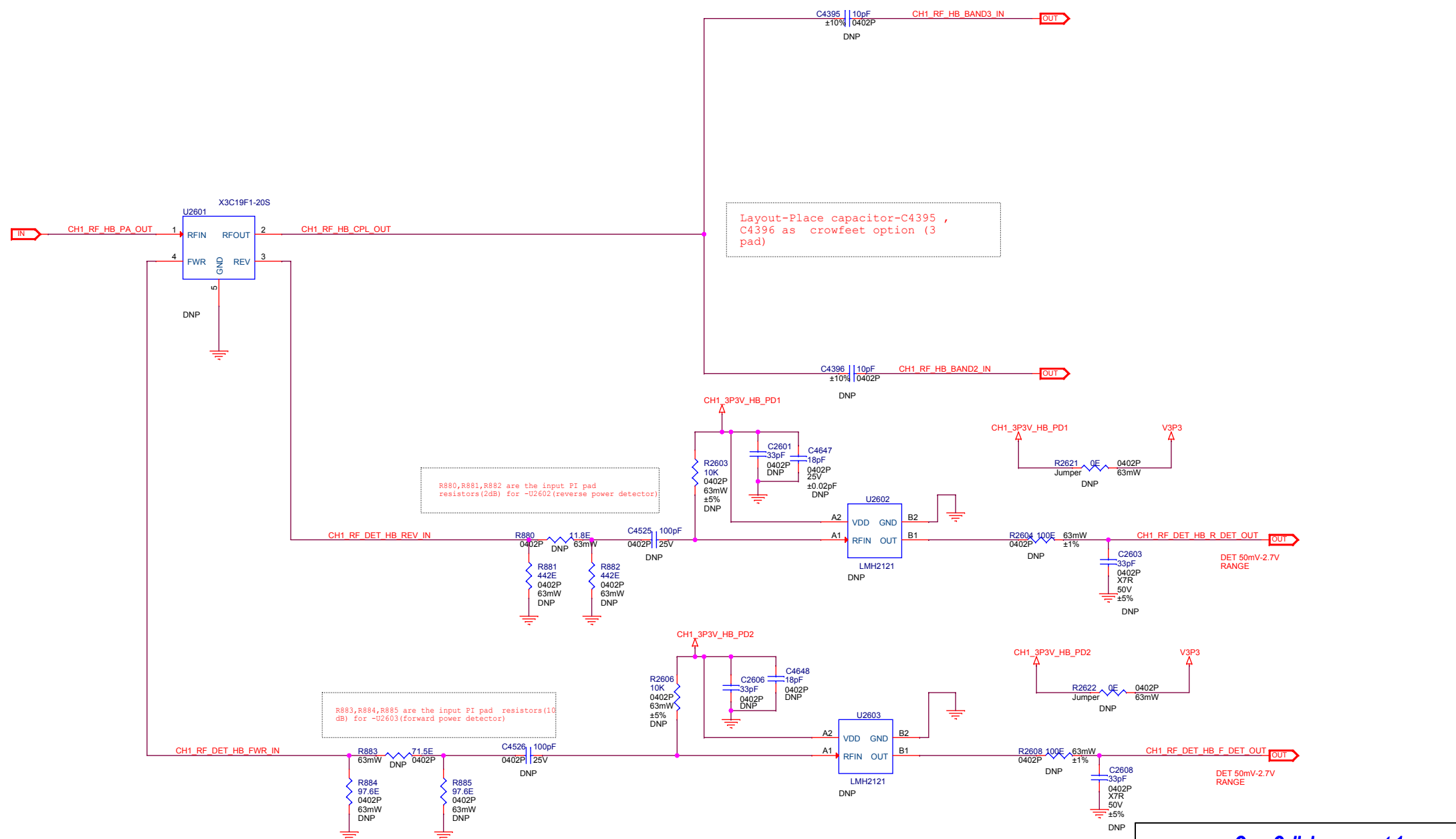
OpenCellular connect-1		
Title CH1_RF_PA_HB		
Size A3	Document Number 00	Rev 1.0
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CH1_ANT_INTERFACE_LB



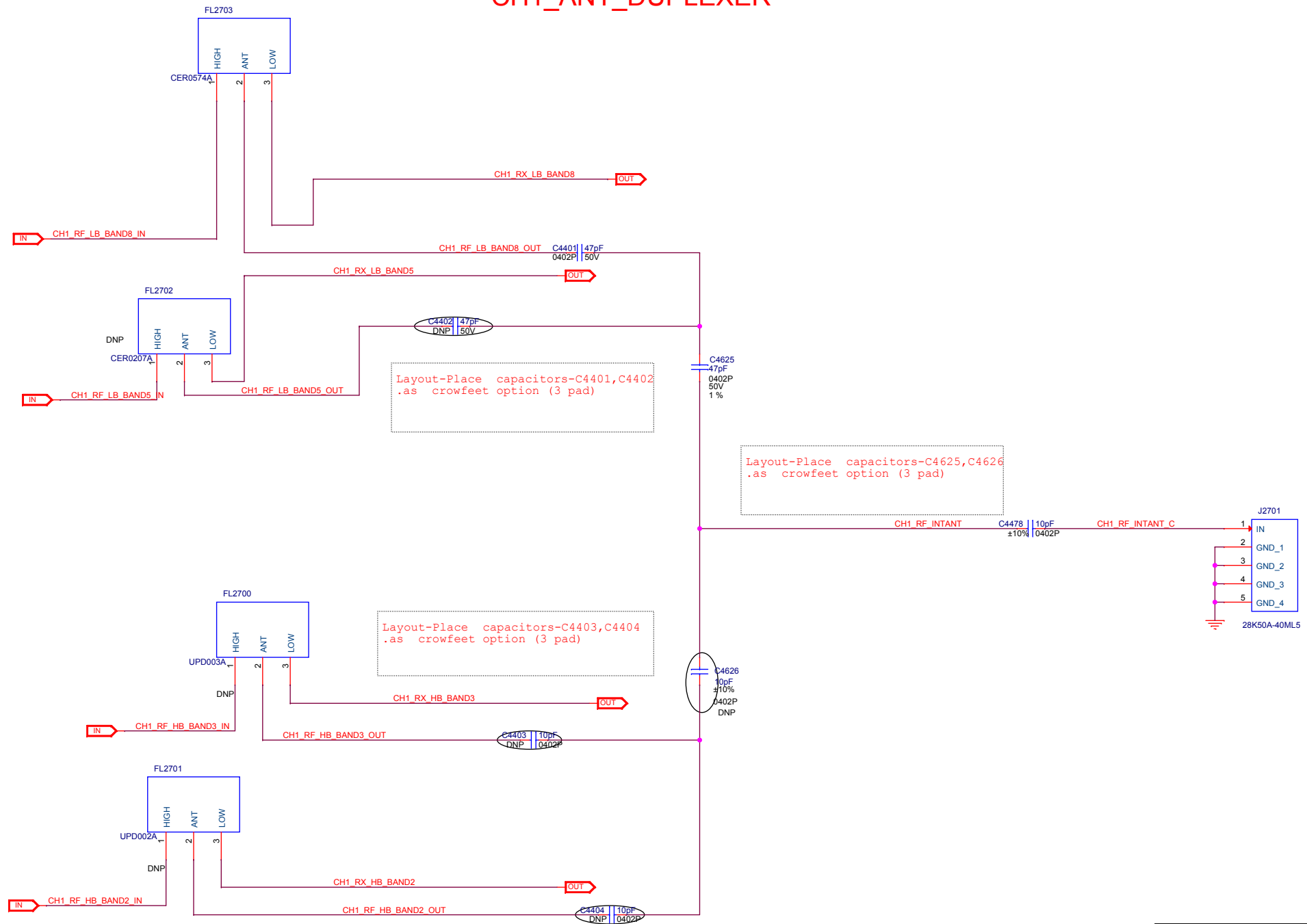
OpenCellular connect-1		
Title CH1_ANT_INTERFACE_LB		
Size A3	Document Number 00	Rev 1.0
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CH1_ANT_INTERFACE_HB



OpenCellular connect-1		
Title		
CH1_ANT_INTERFACE_HB		
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A3	00	1.0
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CH1_ANT_DUPLEXER



Layout-Place capacitors-C4401,C4402
.as crowfeet option (3 pad)

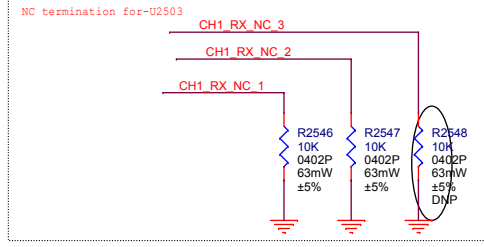
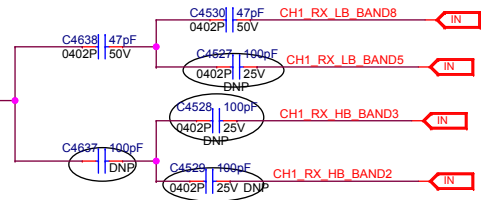
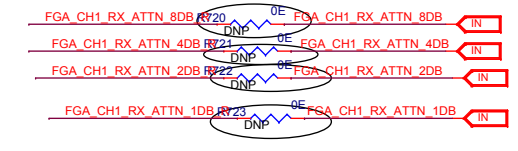
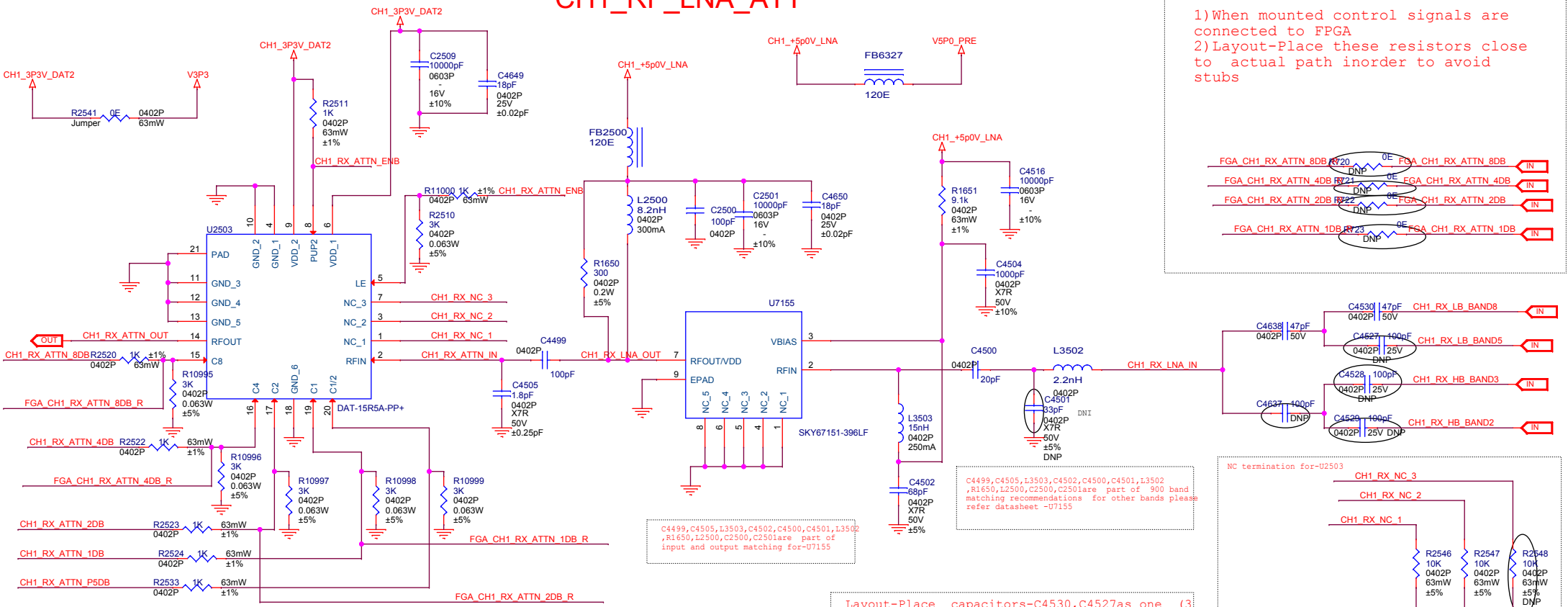
Layout-Place capacitors-C4625,C4626
.as crowfeet option (3 pad)

Layout-Place capacitors-C4403,C4404
.as crowfeet option (3 pad)

OpenCellular connect-1		
Title		
CH1_ANT_DUPLEXER		
Size	Document Number	Rev
A3	00	1.0
Date:	Thursday, December 01, 2016	Sheet 17 of 41

CH1_RF_LNA_ATT

1) When mounted control signals are connected to FPGA
 2) Layout-Place these resistors close to actual path in order to avoid stubs

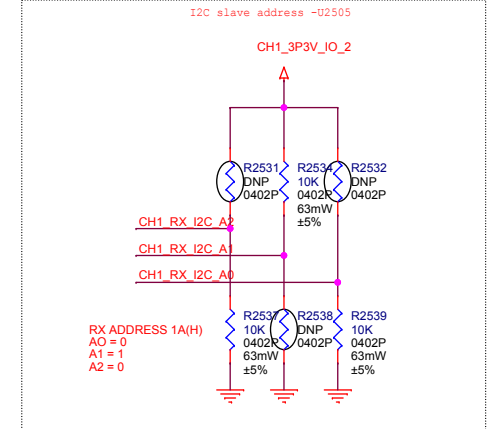
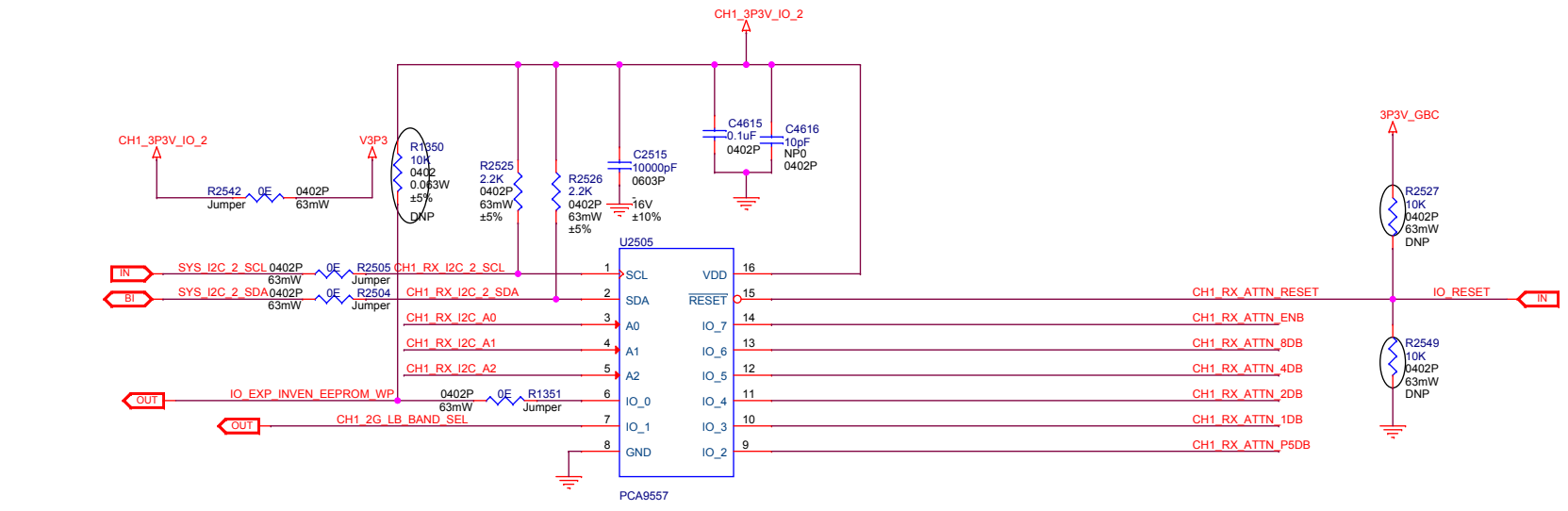


C4499, C4505, L3503, C4502, C4500, C4501, L3502, R1650, L2500, C2500, C2501 are part of input and output matching for U7155

C4499, C4505, L3503, C4502, C4500, C4501, L3502, R1650, L2500, C2500, C2501 are part of 900 band matching recommendations for other bands please refer datasheet -U7155

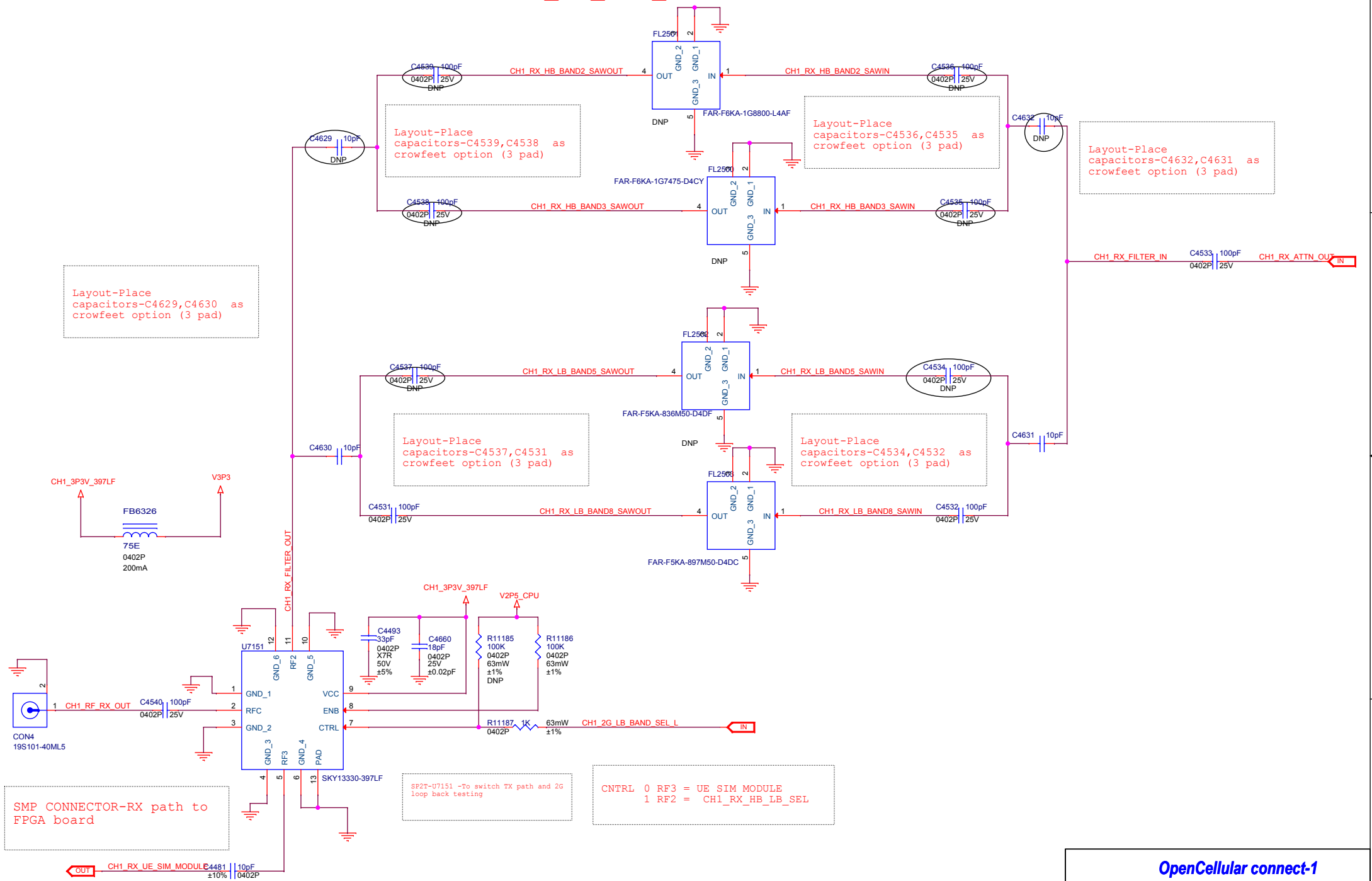
Layout-Place capacitors-C4530, C4527 as one (3 pad), C4528, C4529 as one (3 pad) C4638, C4637 as crowfoot option (3 pad)

- 1) R1650, L2500, R1651 are for VDD and VBIAAS power supply-U7155
- 2) C2500, C2501, C4516, C4504 are decoupling capacitors.-U7155



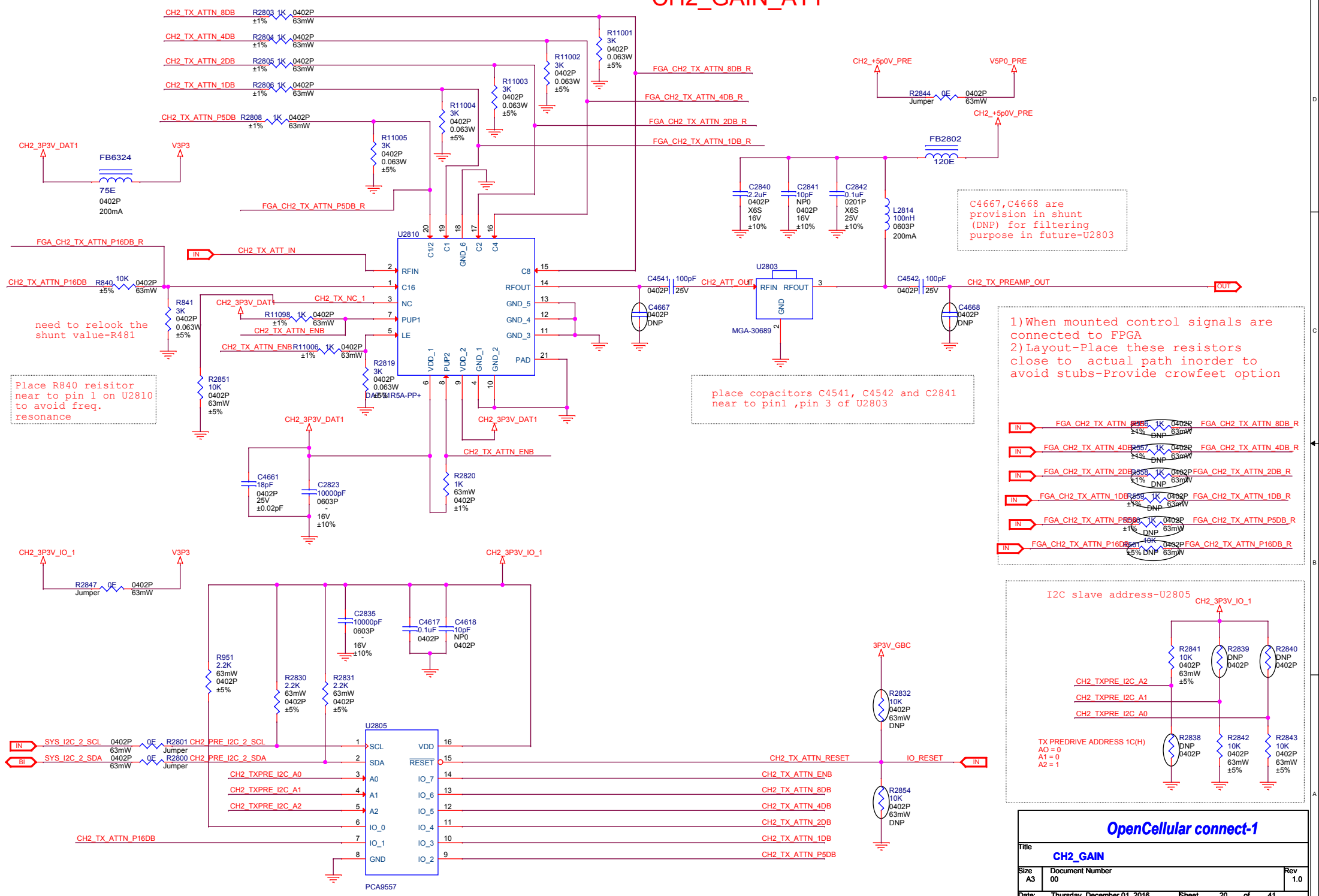
OpenCellular connect-1		
Title	CH1_RF_LNA_1	
Size A3	Document Number 00	Rev 1.0
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CH1_RF_LNA_SAWFILTERS



OpenCellular connect-1		
Title CH1_RF_LNA_SAW FILTERS		
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CH2_GAIN_ATT



CH2_3P3V_DAT1
FB6324
75E
0402P
200mA

FGA CH2 TX ATTN P16DB R

need to relook the shunt value-R481

Place R840 resistor near to pin 1 on U2810 to avoid freq. resonance

CH2_3P3V_IO_1
R2847 Jumper
0402P
63mW

SYS I2C 2_SCL
0402P
63mW

SYS I2C 2_SDA
0402P
63mW

CH2 TX ATTN P16DB

CH2 TX ATTN_8DB R2803 1K 0402P 63mW ±1%

CH2 TX ATTN_4DB R2804 1K 0402P 63mW ±1%

CH2 TX ATTN_2DB R2805 1K 0402P 63mW ±1%

CH2 TX ATTN_1DB R2806 1K 0402P 63mW ±1%

CH2 TX ATTN_P5DB R2808 1K 0402P 63mW ±1%

FGA CH2 TX ATTN_8DB R

FGA CH2 TX ATTN_4DB R

FGA CH2 TX ATTN_2DB R

FGA CH2 TX ATTN_1DB R

FGA CH2 TX ATTN_P5DB R

CH2 TX ATT_IN

CH2_3P3V_DAT1

CH2 TX NC_1

CH2 TX ATTN_ENB

CH2 TX ATTN_ENBR11006

R841 3K 0402P 0.063W ±5%

R11098 1K 0402P 63mW ±1%

R2819 3K 0402P 0.063W ±5%

CH2_3P3V_DAT1

CH2 TX ATTN_ENB

CH2_3P3V_DAT1

CH2_3P3V_IO_1

CH2_3P3V_IO_1

CH2 TXPRE I2C_A0

CH2 TXPRE I2C_A1

CH2 TXPRE I2C_A2

CH2 TX ATTN P16DB

CH2 TX ATTN RESET

CH2 TX ATTN_ENB

CH2 TX ATTN_8DB

CH2 TX ATTN_4DB

CH2 TX ATTN_2DB

CH2 TX ATTN_1DB

CH2 TX ATTN_P5DB

IO_RESET

PCA9557

R11001 3K 0402P 0.063W ±5%

R11002 3K 0402P 0.063W ±5%

R11003 3K 0402P 0.063W ±5%

R11004 3K 0402P 0.063W ±5%

R11005 3K 0402P 0.063W ±5%

CH2 +5p0V_PRE

V5P0_PRE

R2844 Jumper 0E 0402P 63mW

FB2802 120E

CH2 ATT_OUT

U2803

MGA-30689

CH2 TX PREAMP OUT

OUT

place capacitors C4541, C4542 and C2841 near to pin1 ,pin 3 of U2803

CH2_3P3V_DAT1

CH2 TX ATTN_ENB

CH2_3P3V_DAT1

CH2_3P3V_IO_1

CH2_3P3V_IO_1

CH2 TXPRE I2C_A2

CH2 TXPRE I2C_A1

CH2 TXPRE I2C_A0

CH2 TX ATTN P16DB

CH2 TX ATTN RESET

CH2 TX ATTN_ENB

CH2 TX ATTN_8DB

CH2 TX ATTN_4DB

CH2 TX ATTN_2DB

CH2 TX ATTN_1DB

CH2 TX ATTN_P5DB

IO_RESET

PCA9557

R2803 1K 0402P 63mW ±1%

R2804 1K 0402P 63mW ±1%

R2805 1K 0402P 63mW ±1%

R2806 1K 0402P 63mW ±1%

R2808 1K 0402P 63mW ±1%

FGA CH2 TX ATTN_8DB R

FGA CH2 TX ATTN_4DB R

FGA CH2 TX ATTN_2DB R

FGA CH2 TX ATTN_1DB R

FGA CH2 TX ATTN_P5DB R

CH2 TX ATT_IN

CH2_3P3V_DAT1

CH2 TX NC_1

CH2 TX ATTN_ENB

CH2 TX ATTN_ENBR11006

R841 3K 0402P 0.063W ±5%

R11098 1K 0402P 63mW ±1%

R2819 3K 0402P 0.063W ±5%

CH2_3P3V_DAT1

CH2 TX ATTN_ENB

CH2_3P3V_DAT1

CH2_3P3V_IO_1

CH2_3P3V_IO_1

CH2 TXPRE I2C_A2

CH2 TXPRE I2C_A1

CH2 TXPRE I2C_A0

CH2 TX ATTN P16DB

CH2 TX ATTN RESET

CH2 TX ATTN_ENB

CH2 TX ATTN_8DB

CH2 TX ATTN_4DB

CH2 TX ATTN_2DB

CH2 TX ATTN_1DB

CH2 TX ATTN_P5DB

IO_RESET

PCA9557

R11001 3K 0402P 0.063W ±5%

R11002 3K 0402P 0.063W ±5%

R11003 3K 0402P 0.063W ±5%

R11004 3K 0402P 0.063W ±5%

R11005 3K 0402P 0.063W ±5%

CH2 +5p0V_PRE

V5P0_PRE

R2844 Jumper 0E 0402P 63mW

FB2802 120E

CH2 ATT_OUT

U2803

MGA-30689

CH2 TX PREAMP OUT

OUT

place capacitors C4541, C4542 and C2841 near to pin1 ,pin 3 of U2803

CH2_3P3V_DAT1

CH2 TX ATTN_ENB

CH2_3P3V_DAT1

CH2_3P3V_IO_1

CH2_3P3V_IO_1

CH2 TXPRE I2C_A2

CH2 TXPRE I2C_A1

CH2 TXPRE I2C_A0

CH2 TX ATTN P16DB

CH2 TX ATTN RESET

CH2 TX ATTN_ENB

CH2 TX ATTN_8DB

CH2 TX ATTN_4DB

CH2 TX ATTN_2DB

CH2 TX ATTN_1DB

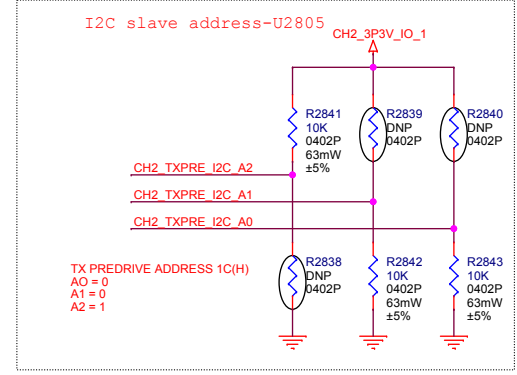
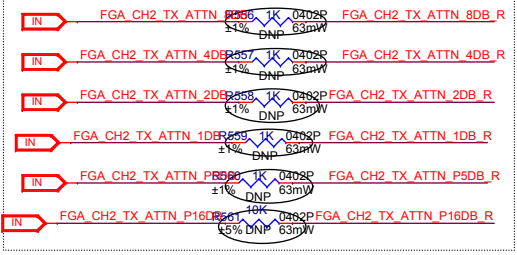
CH2 TX ATTN_P5DB

IO_RESET

PCA9557

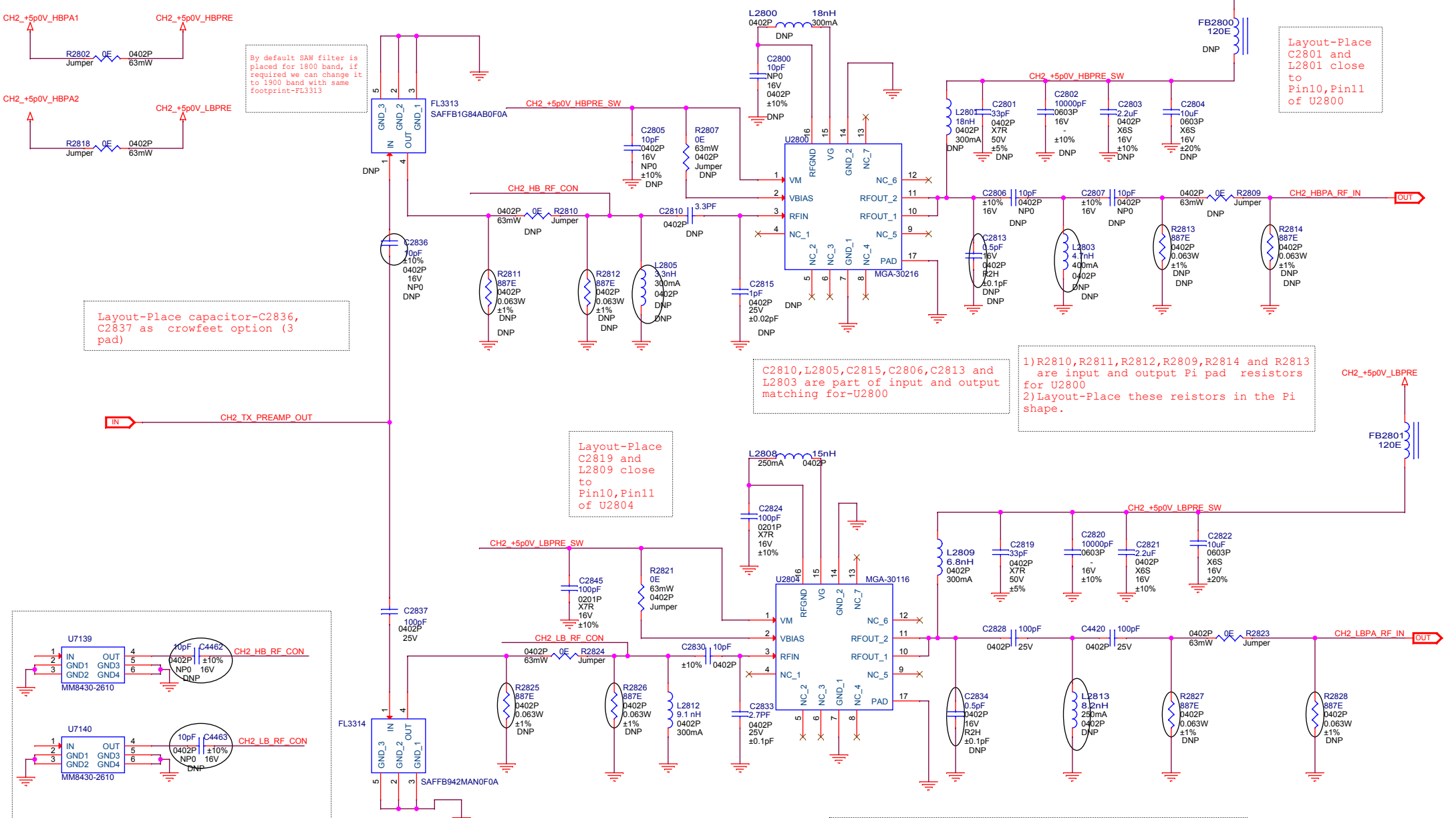
C4667, C4668 are provision in shunt (DNP) for filtering purpose in future-U2803

- 1) When mounted control signals are connected to FPGA
- 2) Layout-Place these resistors close to actual path in order to avoid stubs-Provide crowfoot option



OpenCellular connect-1		
Title CH2_GAIN		
Size A3	Document Number 00	Rev 1.0
Date: Thursday, December 01, 2016	Sheet 20	of 41

CH2_RF_PA_PREDRIVE



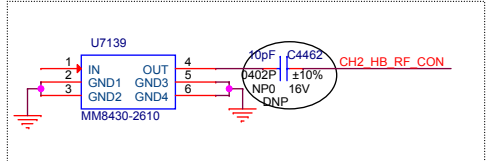
By default SAW filter is placed for 1800 band, if required we can change it to 1900 band with same footprint-FL3313

Layout-Place capacitor-C2836, C2837 as crowfeet option (3 pad)

C2810, L2805, C2815, C2806, C2813 and L2803 are part of input and output matching for-U2800

1) R2810, R2811, R2812, R2809, R2814 and R2813 are input and output Pi pad resistors for U2800
2) Layout-Place these resistors in the Pi shape.

Layout-Place C2819 and L2809 close to Pin10, Pin11 of U2804



Layout-Place DNP capacitor as crowfeet option (3 pad) near to R2810, R2824 respectively

By default SAW filter is placed for 900 band, if required we can change it to 850 band with same footprint-FL3314

C2830, L2812, C2833, C2834, C2828 and L2813 are part of input and output matching for-U2804

1) R2824, R2825, R2826, R2823, R2827 and R2828 are input and output Pi pad resistors for U2804
2) Layout-Place these resistors in the Pi shape.

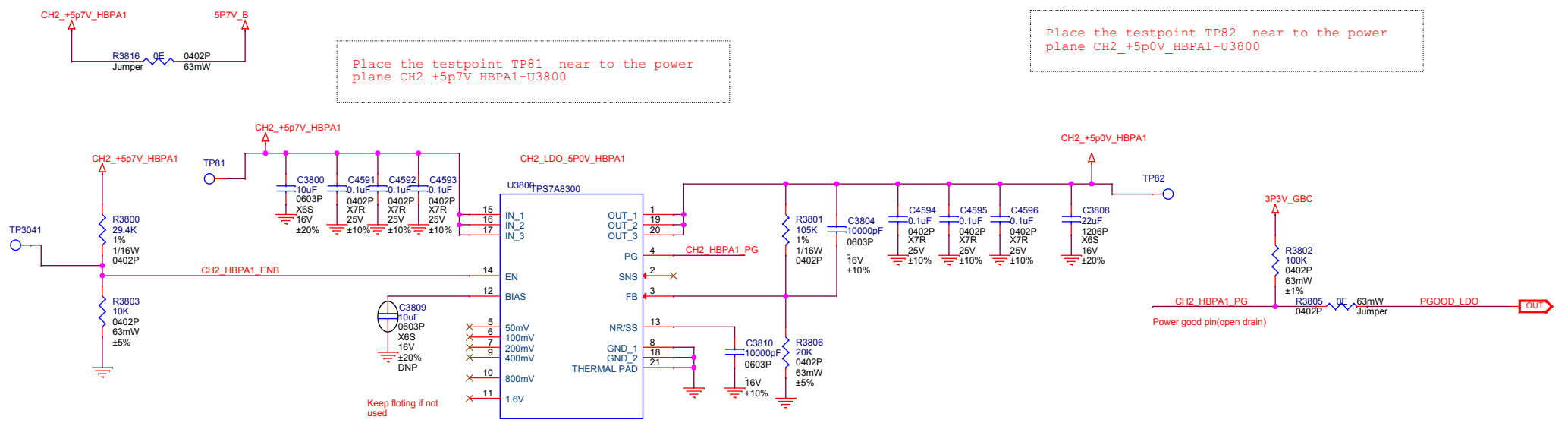
Layout-Place C2801 and L2801 close to Pin10, Pin11 of U2800

OpenCellular connect-1		
Title		
CH2_RF_PA_PREDRIVE		
Size	Document Number	Rev
A3		1.0
Date:	Thursday, December 01, 2016	Sheet 21 of 41

CH2_HB_LDO

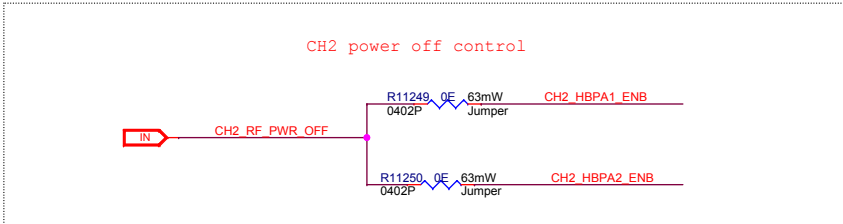
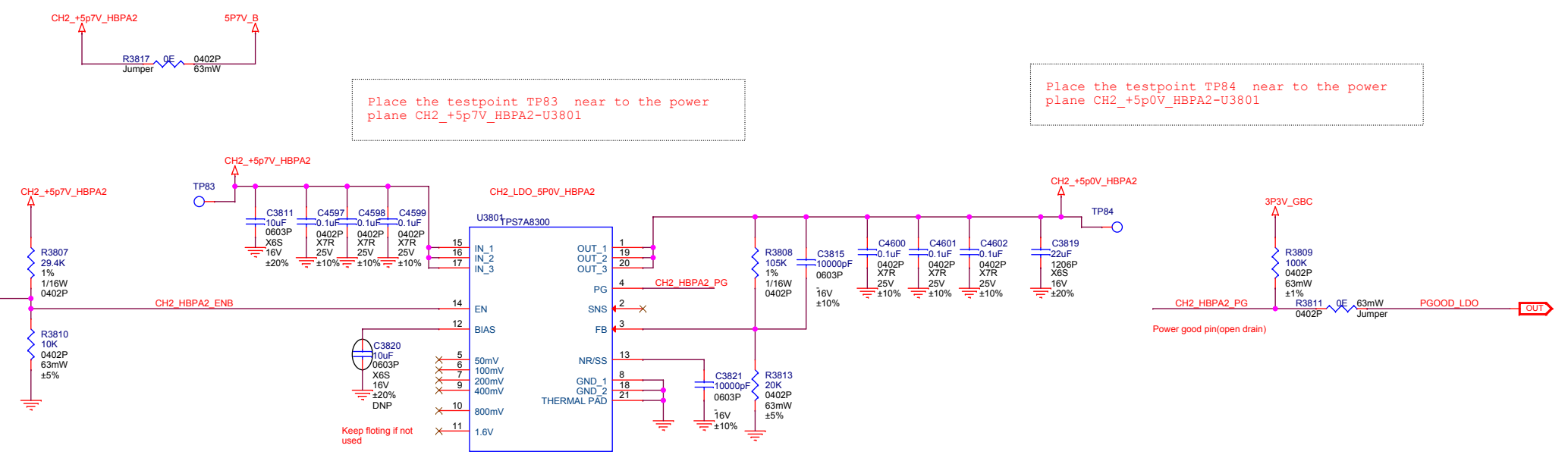
Place the testpoint TP82 near to the power plane CH2_+5p0V_HBPA1-U3800

Place the testpoint TP81 near to the power plane CH2_+5p7V_HBPA1-U3800



Place the testpoint TP84 near to the power plane CH2_+5p0V_HBPA2-U3801

Place the testpoint TP83 near to the power plane CH2_+5p7V_HBPA2-U3801



OpenCellular connect-1		
Title CH2_HB_LDO		
Size A3	Document Number 00	Rev 1.0
Date: Thursday, December 01, 2016	Sheet 22	of 41

CH2_RF_PA_LB

Layout-Place DNP capacitor-C4453 as crowfeet option (3 pad) near to C4455

Layout-1)Place C3003 capacitor near to pin 20 of -U3000
2)Place C3004 capacitor near to pin 18 of U3000

R865,R866,R867 are the PI pad resistors for the ISO port of-U3003

R11171,R11175,R11174 are the 2dB PI pad resistors for the input port of-U3000

L3000,C3010,L3002,C3013,C4423,C3014,C4471,L3003 are part of input and output matching for-U3000

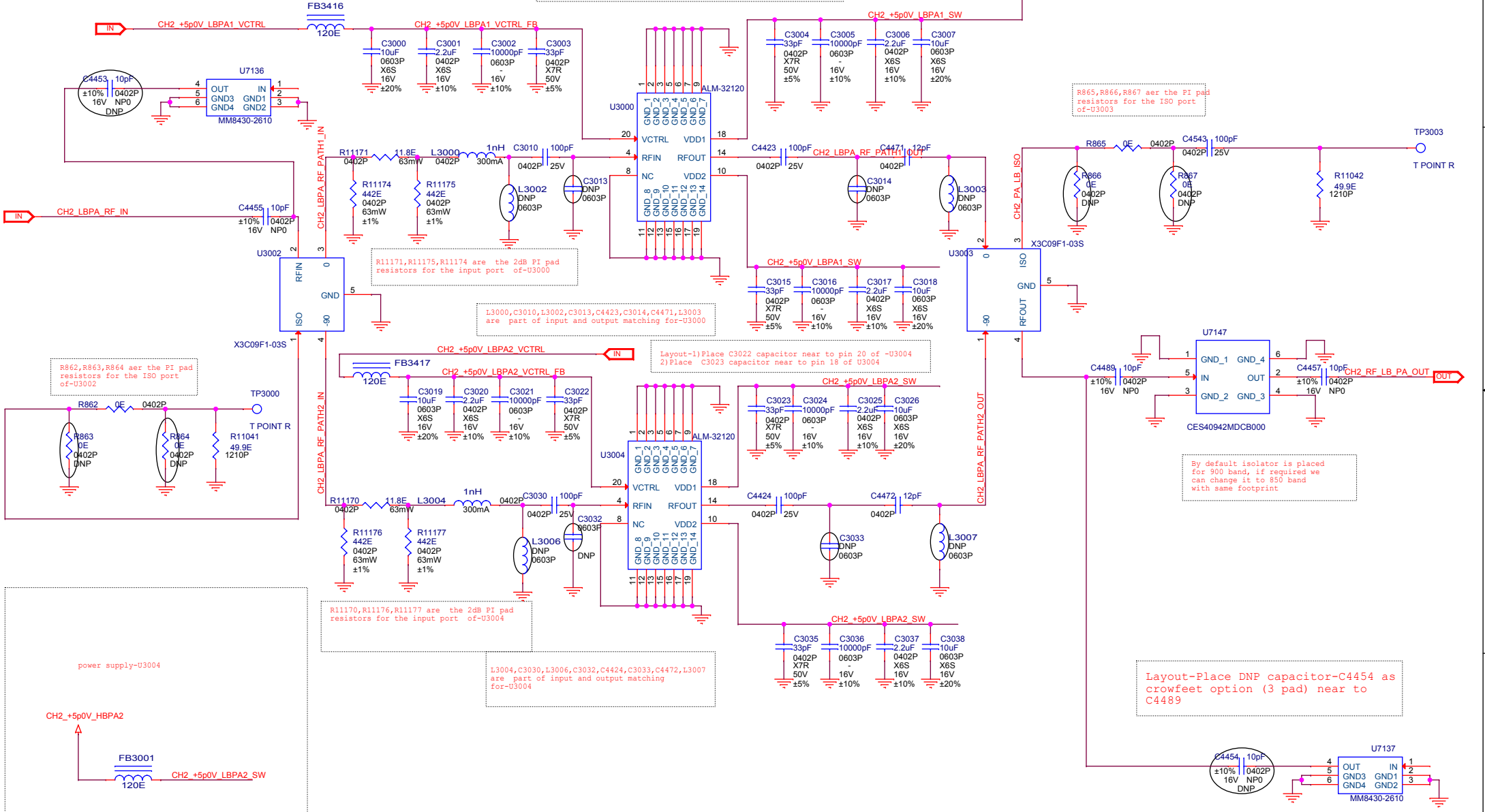
Layout-1)Place C3022 capacitor near to pin 20 of -U3004
2)Place C3023 capacitor near to pin 18 of U3004

By default isolator is placed for 900 band, if required we can change it to 850 band with same footprint

R11170,R11176,R11177 are the 2dB PI pad resistors for the input port of-U3004

L3004,C3030,L3006,C3032,C4424,C3033,C4472,L3007 are part of input and output matching for-U3004

Layout-Place DNP capacitor-C4454 as crowfeet option (3 pad) near to C4489



power supply-U3004

OpenCellular connect-1		
CH2_RF_PA_LB		
Title	CH2_RF_PA_LB	
Size A3	Document Number	Rev
00	00	1.0
Date:	Thursday, December 01, 2016	Sheet 23 of 41

CH2_RF_PA_HB

Layout-Place DNP capacitor-C4458 as crowfeet option (3 pad) near to C4459

Layout-1)Place C2904 capacitor near to pin 20 of -U2900
2)Place C2905 capacitor near to pin 18 of U2900

R871,R872,R873 aer the PI pad resistors for the ISO port of-U2903

To place a ground plane at 0.3mm from the top surface is recommended-U7149

R868,R869,R870 aer the PI pad resistors for the ISO port of-U2902

Layout-1)Place C2922 capacitor near to pin 20 of -U2904
2)Place C2923 capacitor near to pin 18 of U2904

By default isolator is placed for 1800 band, if required we can change it to 1900 band with same footprint

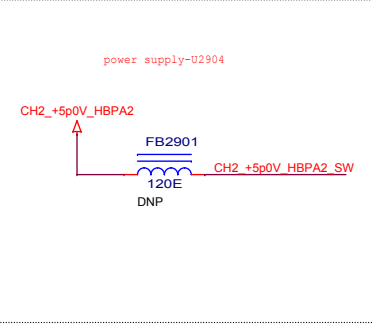
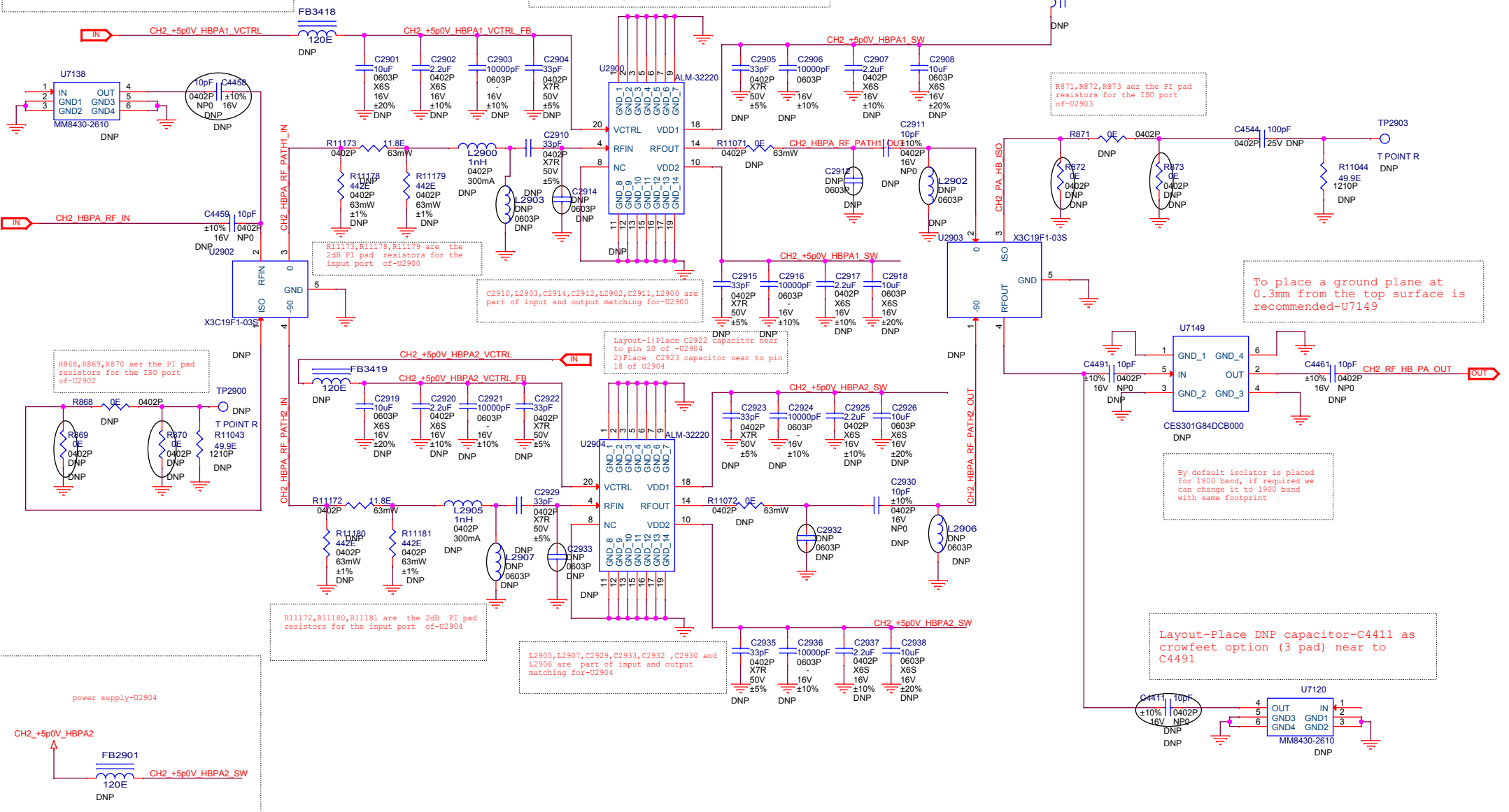
Layout-Place DNP capacitor-C4411 as crowfeet option (3 pad) near to C4491

R11173,R11178,R11179 are the 2dB PI pad resistors for the input port of-U2900

C2910,L2903,C2914,C2912,L2902,C2911,L2900 are part of input and output matching for-U2900

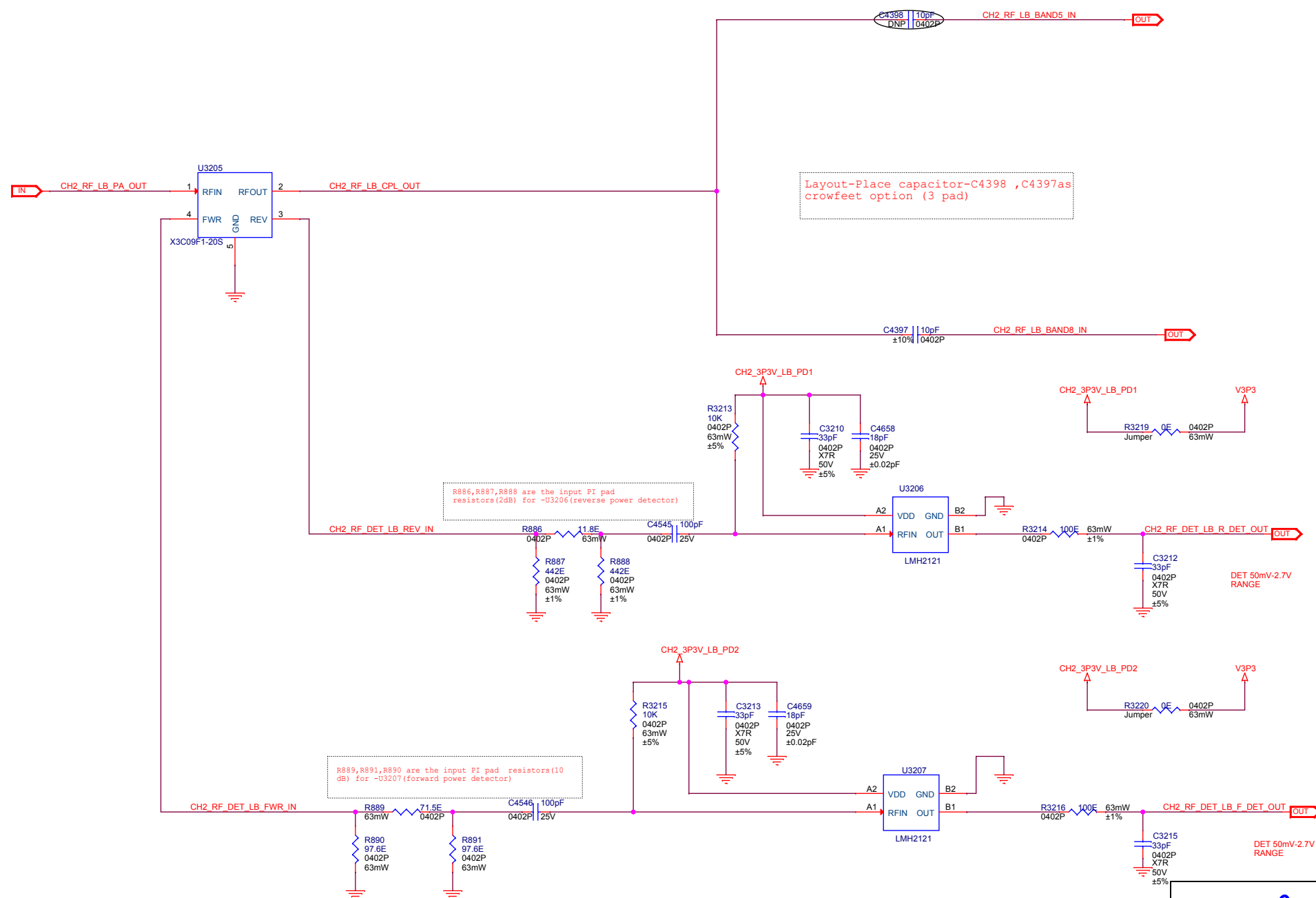
R11172,R11180,R11181 are the 2dB PI pad resistors for the input port of-U2904

L2905,L2907,C2929,C2933,C2932,C2930 and L2906 are part of input and output matching for-U2904



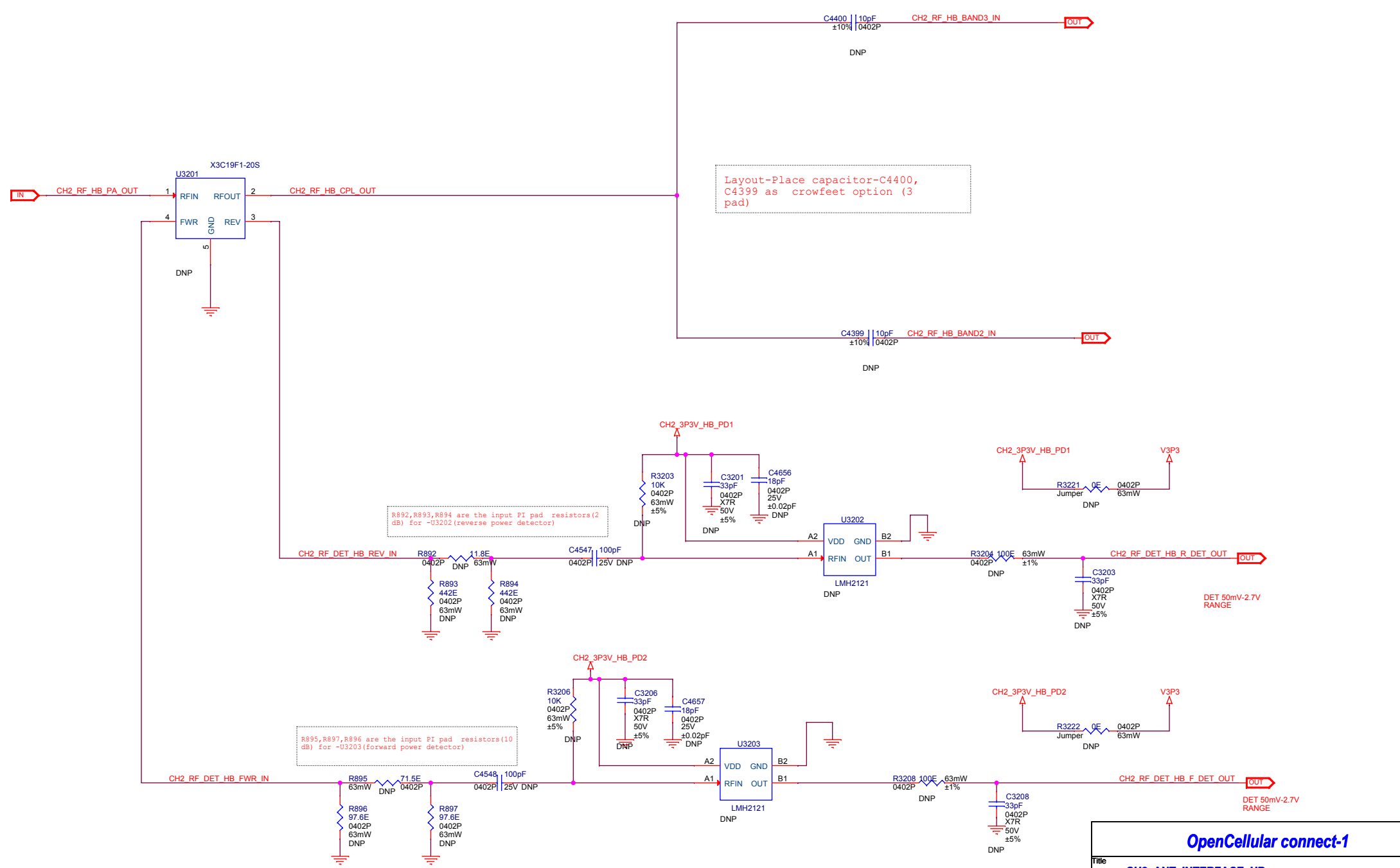
OpenCellular connect-1		
Title CH2_RF_PA_HB		
Size A3	Document Number 00	Rev 1.0
Date: Thursday, December 01, 2016	Sheet 24	of 41

CH2_ANT_INTERFACE_LB



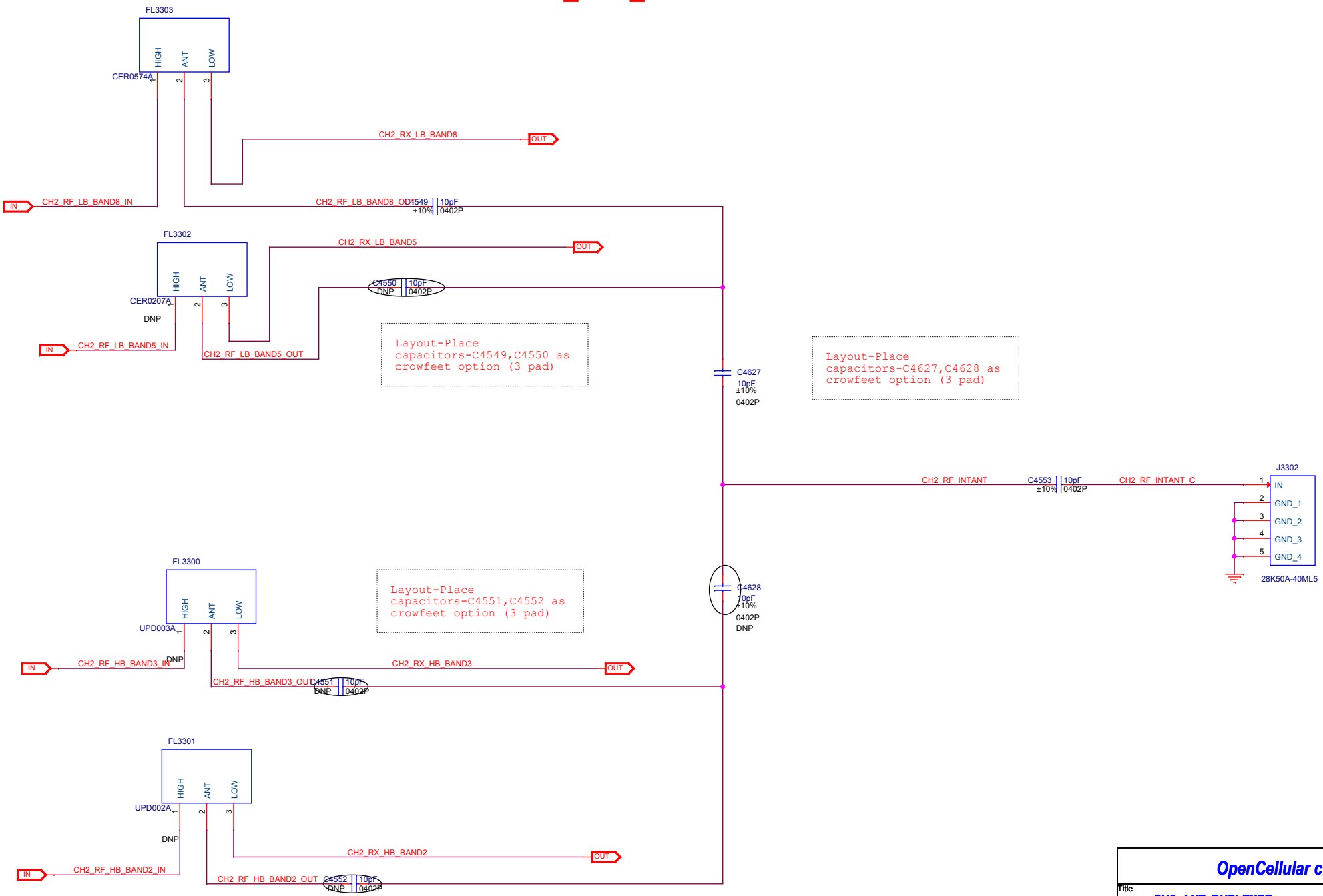
OpenCellular connect-1		
Title		
CH2_ANT_INTERFACE_LB		
Size	Document Number	Rev
A3	00	1.0
Date:	Thursday, December 01, 2016	Sheet 25 of 41

CH2_ANT_INTERFACE_HB



OpenCellular connect-1		
Title		
CH2_ANT_INTERFACE_HB		
Size	Document Number	Rev
A3	00	1.0
Date:	Thursday, December 01, 2016	Sheet 26 of 41

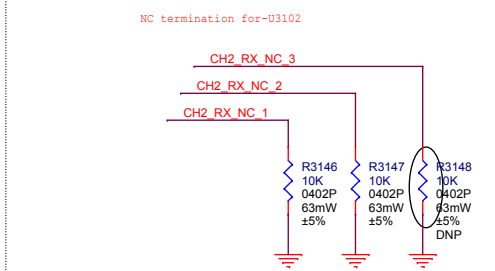
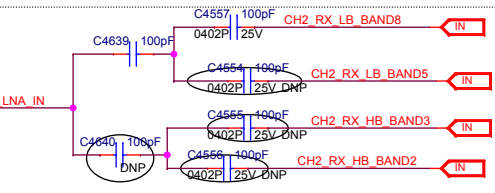
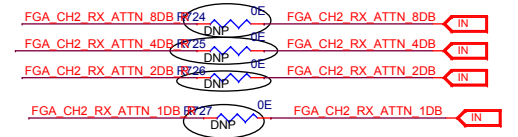
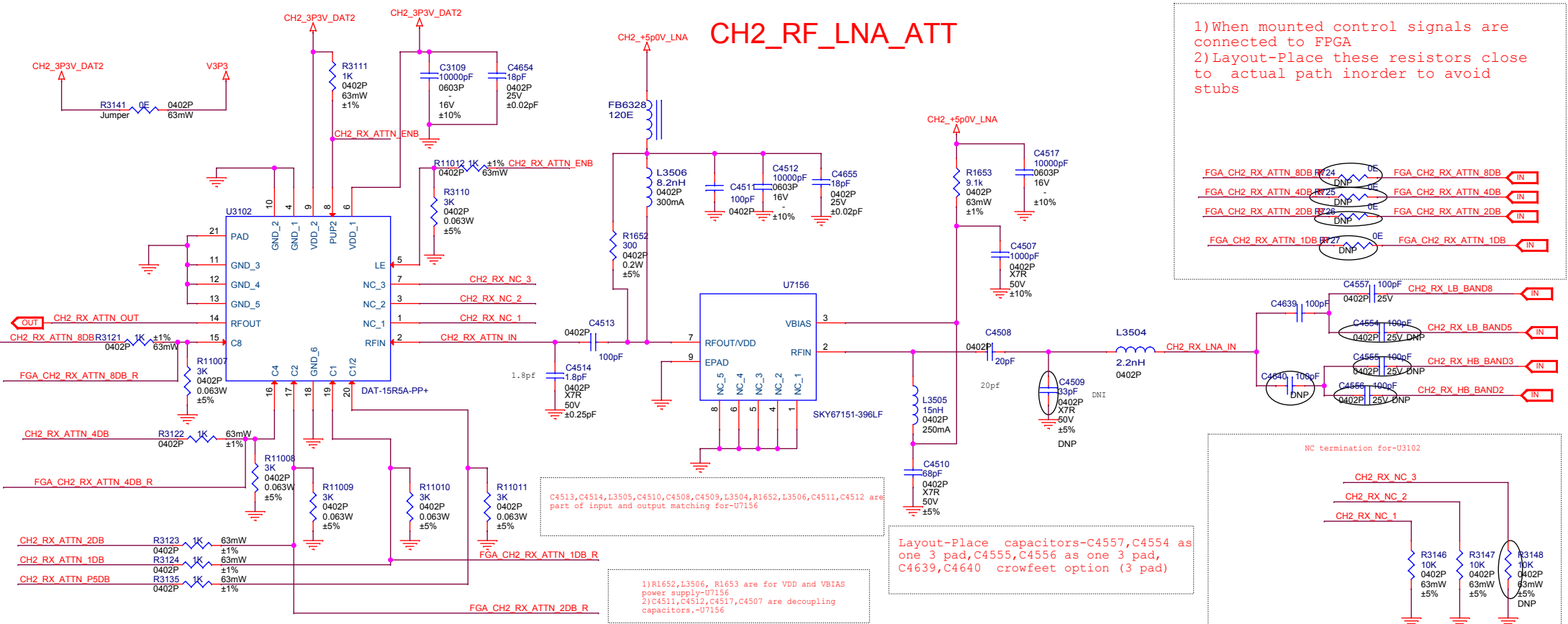
CH2_ANT_DUPLEXER



OpenCellular connect-1		
Title CH2_ANT_DUPLEXER		
Size A3	Document Number 00	Rev 1.0
Date: Thursday, December 01, 2016		
Sheet 27 of 41		

CH2_RF_LNA_ATT

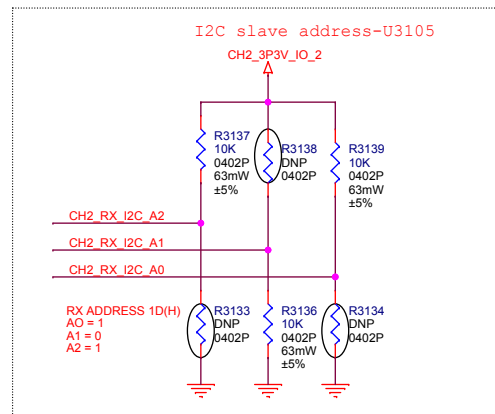
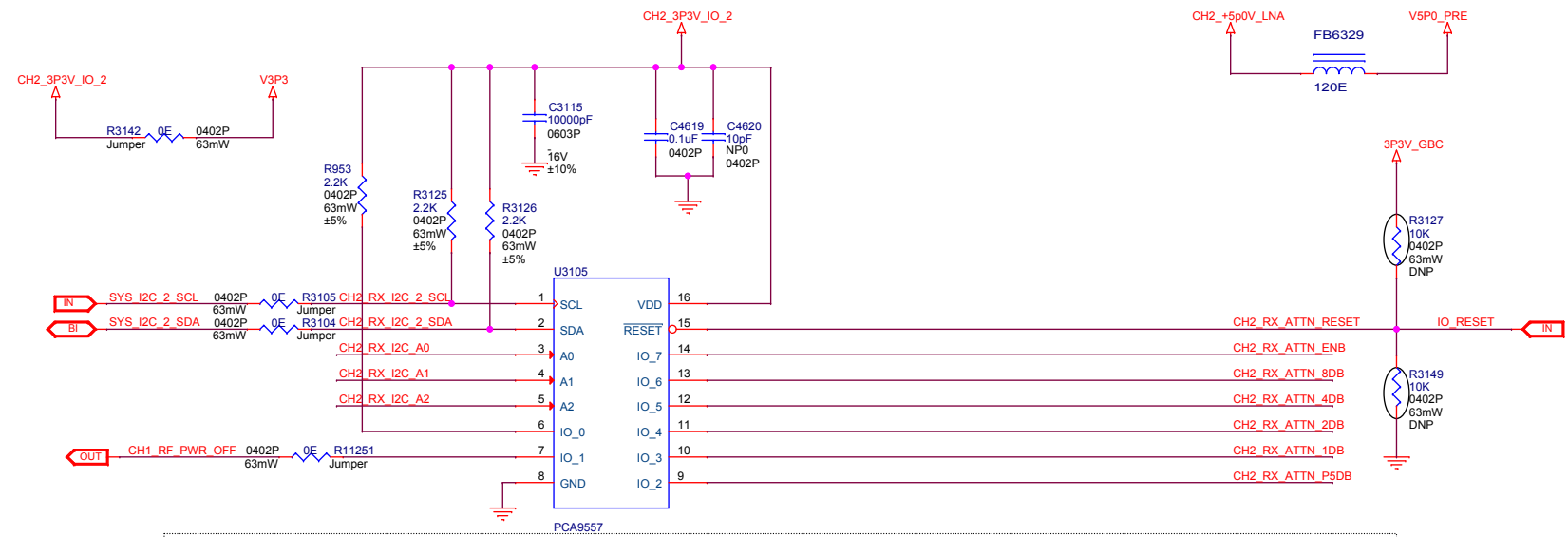
1) When mounted control signals are connected to FPGA
 2) Layout-Place these resistors close to actual path in order to avoid stubs



C4513, C4514, L3505, C4510, C4508, C4509, L3504, R1652, L3506, C4511, C4512 are part of input and output matching for U7156

Layout-Place capacitors-C4557, C4554 as one 3 pad, C4554 as one 3 pad, C4639, C4640 crowfeet option (3 pad)

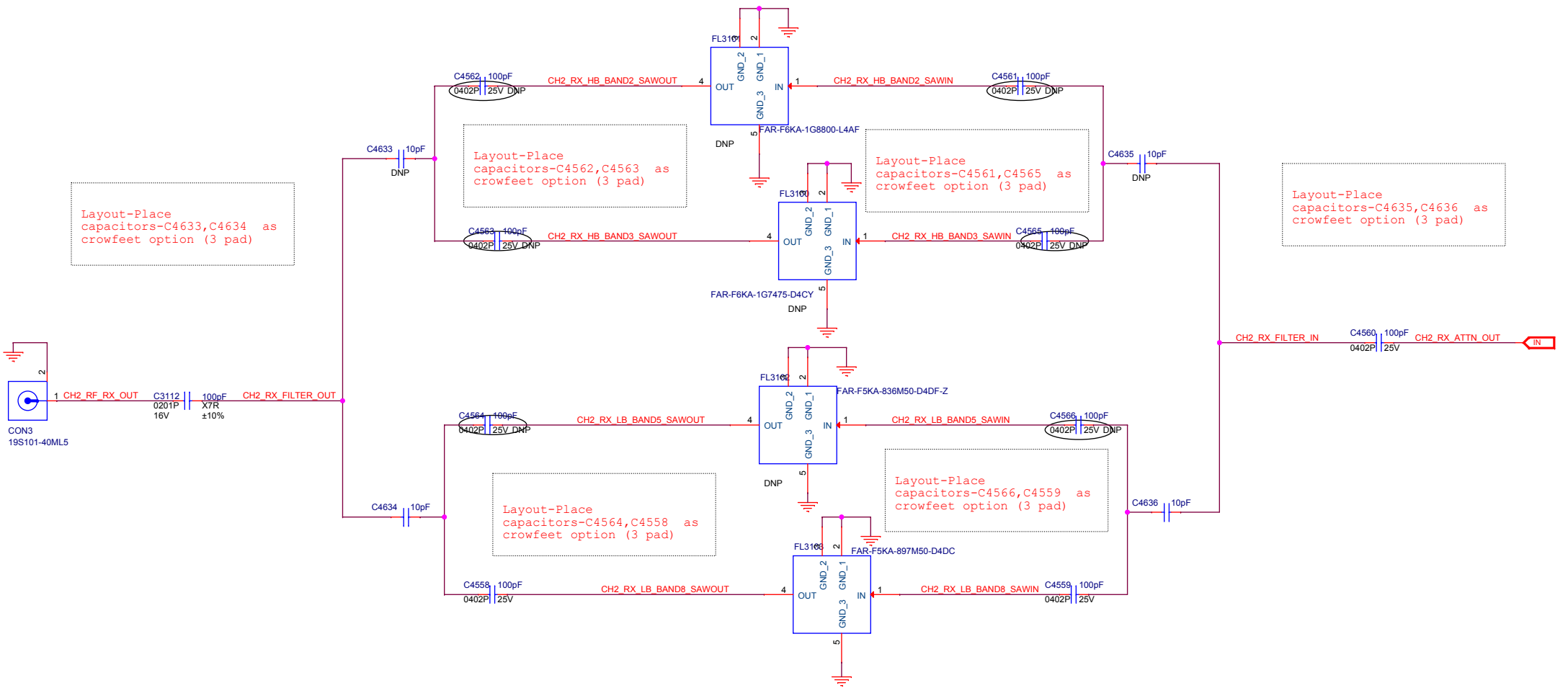
1) R1652, L3506, R1653 are for VDD and VBIAS power supply-U7156
 2) C4511, C4512, C4517, C4507 are decoupling capacitors-U7156



C4513, C4514, L3505, C4510, C4508, C4509, L3504, R1652, L3506, C4511, C4512, R1653, C4507, C4517 are part of 900 band matching recommendations for other bands please refer datasheet-U7156

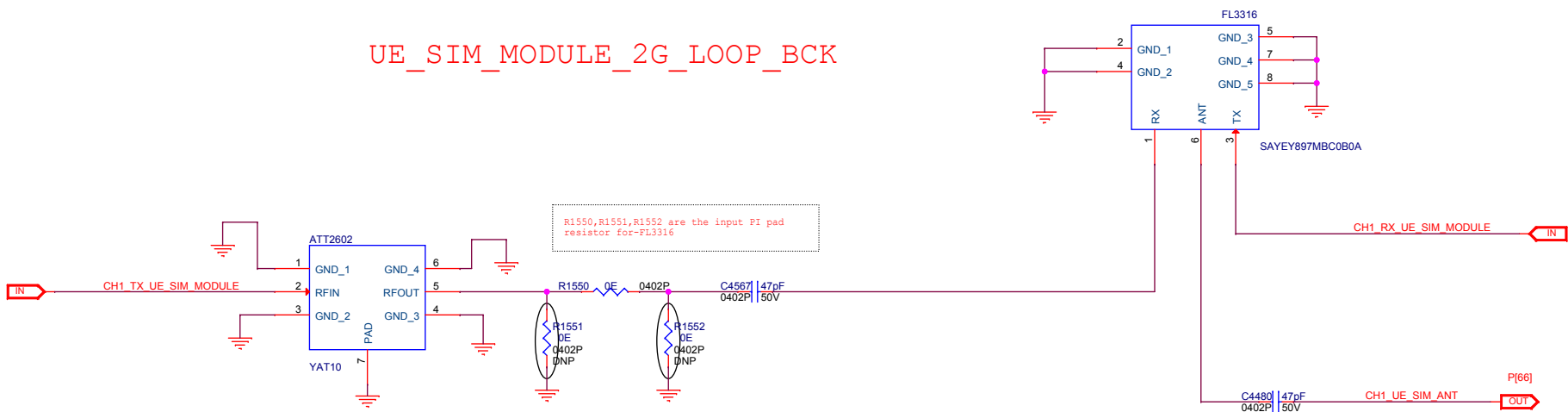
OpenCellular connect-1		
Title	CH2_RF_LNA_1	
Size	Document Number	Rev
A3	00	1.0
Date:	Thursday, December 01, 2016	Sheet 28 of 41

CH2_RF_LNA_SAWFILTERS

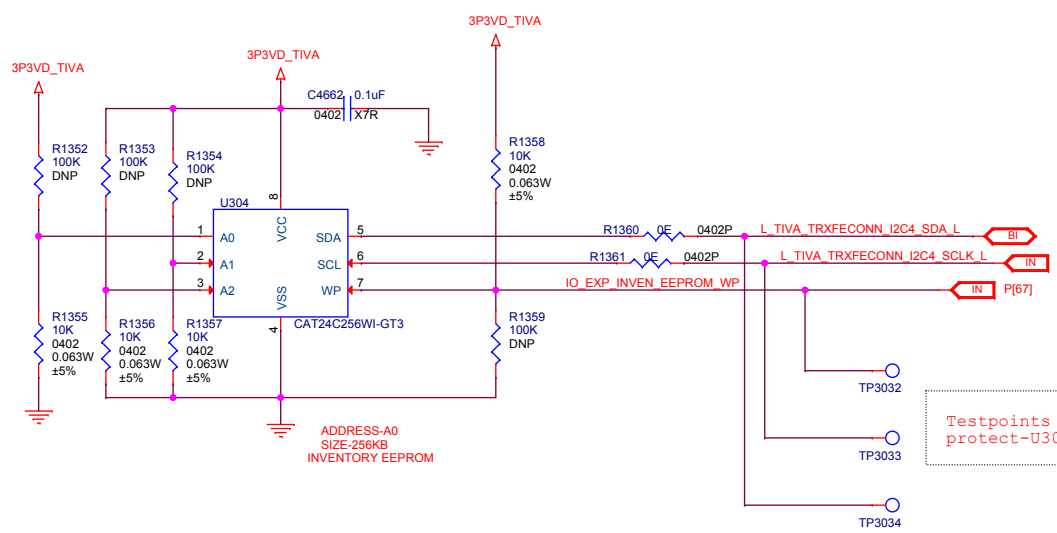


OpenCellular connect-1			
Title CH2_RF_LNA_2			
Size A3	Document Number 00		Rev 1.0
Date: Thursday, December 01, 2016		Sheet 29	of 41

UE_SIM_MODULE_2G_LOOP_BCK

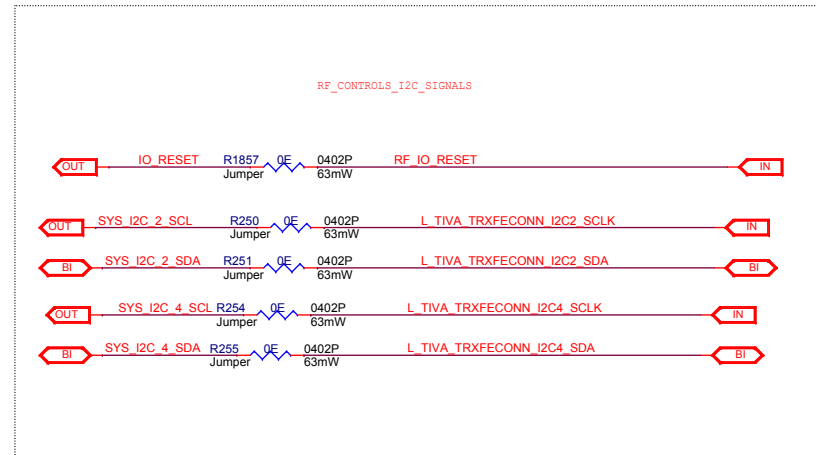
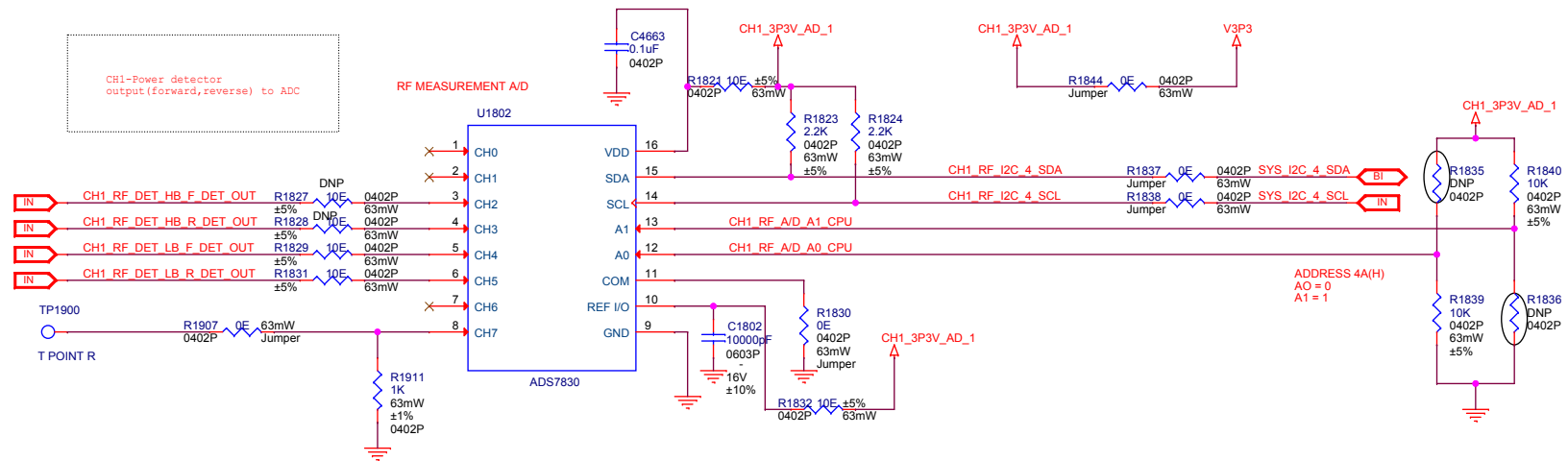


INVENTORY EEPROM-256KB



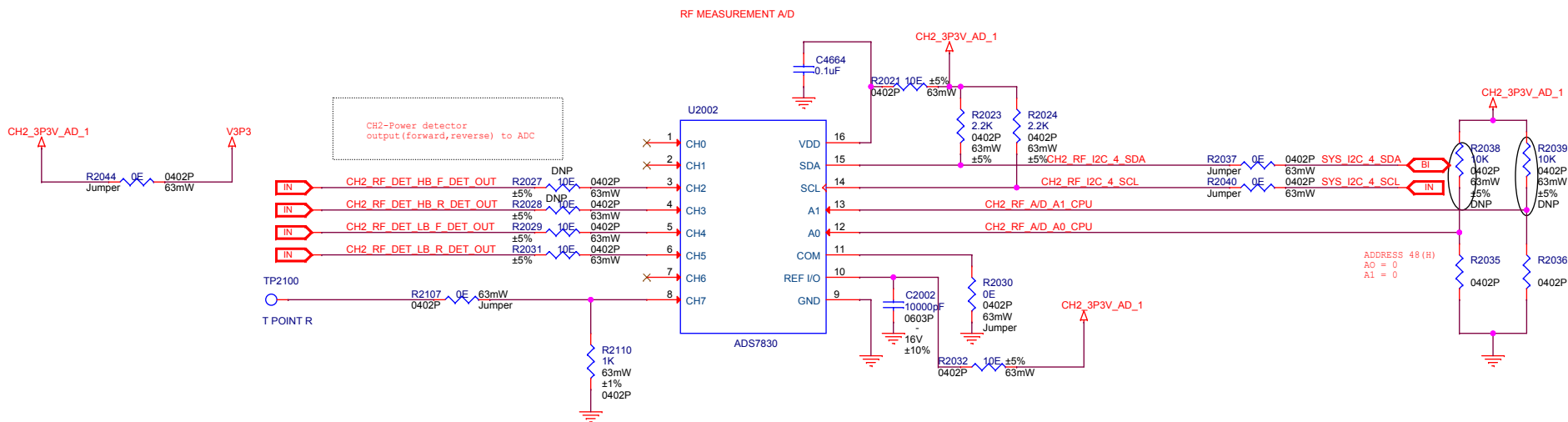
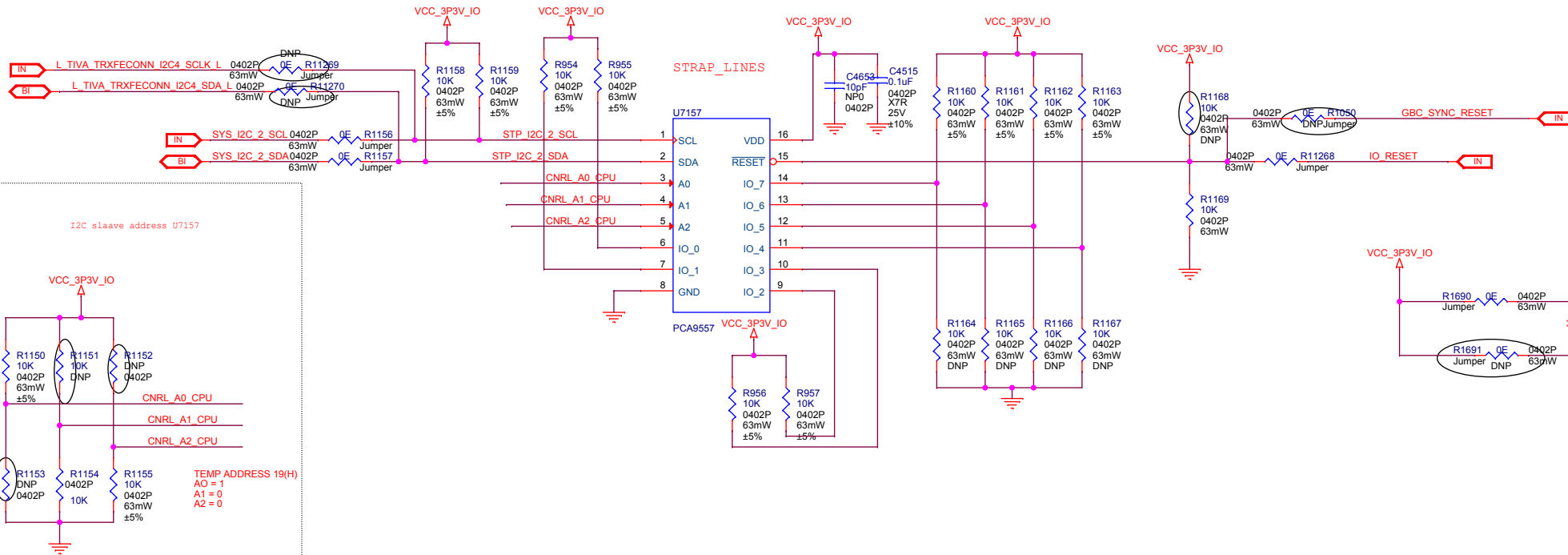
OpenCellular connect-1		
Title		
UE_SIM_MODULE		
Size	Document Number	Rev
A3		1.0
Date:	Thursday, December 01, 2016	Sheet 30 of 41

CONTROL_SECTION_1



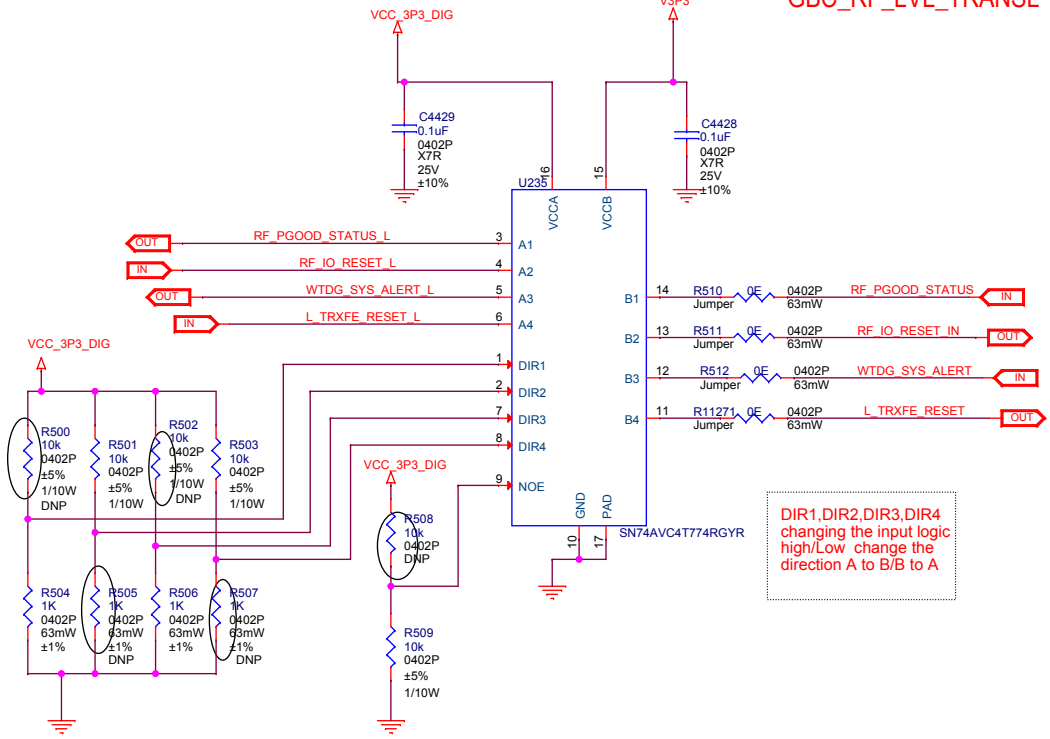
OpenCellular connect-1		
Title		
CH1_CPU_SECTION_1		
Size	Document Number	Rev
A3	00	1.0
Date:	Thursday, December 01, 2016	Sheet 31 of 41

CONTROL_SECTION_2

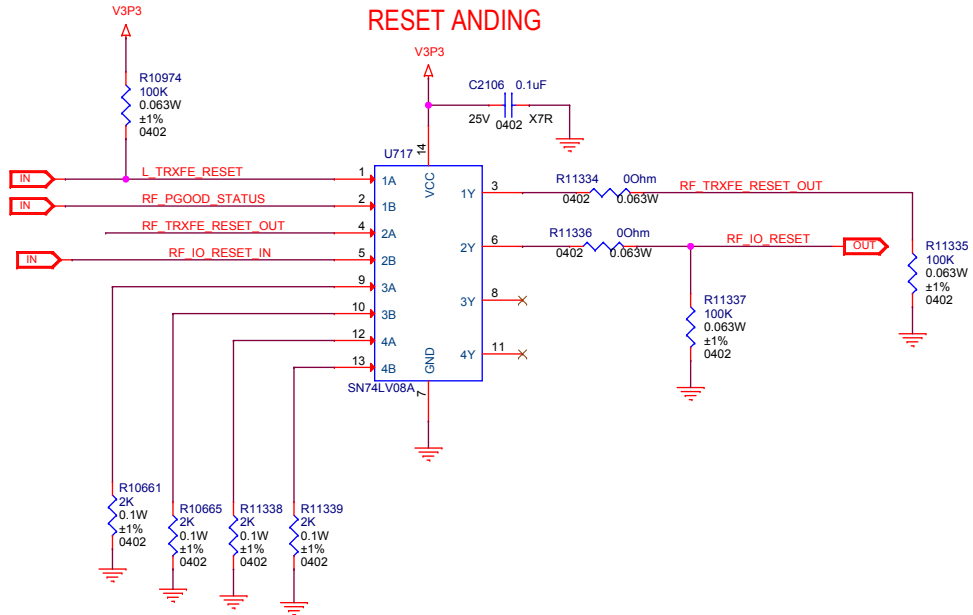


OpenCellular connect-1		
Title	CH2_CPU_SECTION_1	
Size A3	Document Number 00	Rev 1.0
Date:	Thursday, December 01, 2016	Sheet 32 of 41

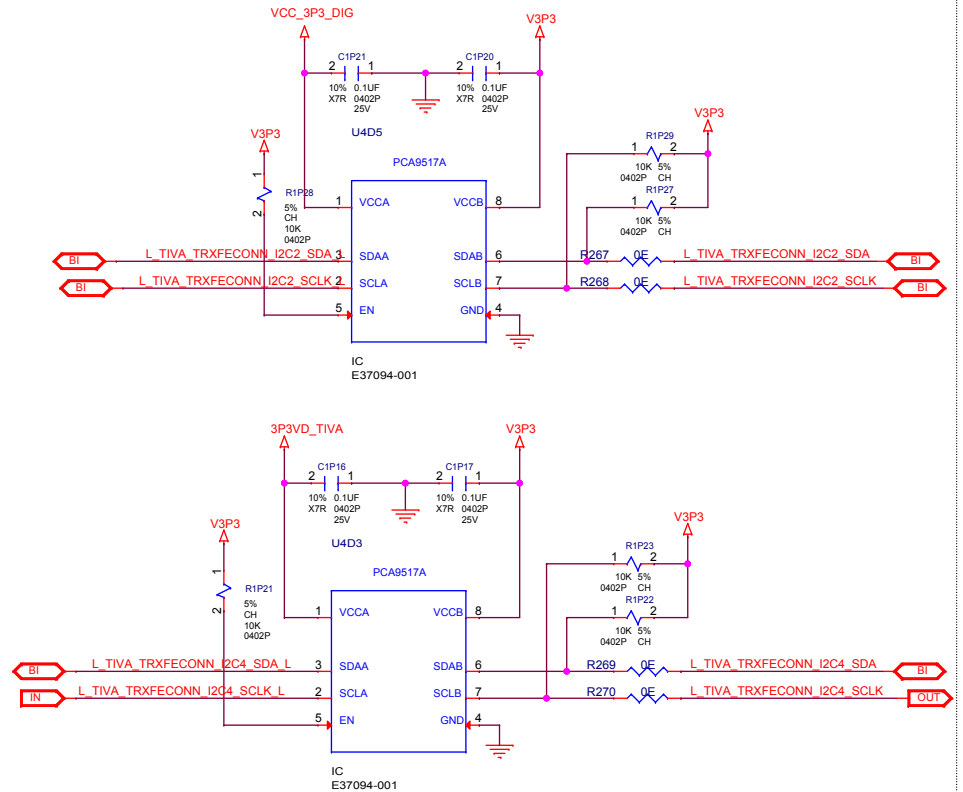
GBC_RF_LVL_TRANSL



RESET ANDING



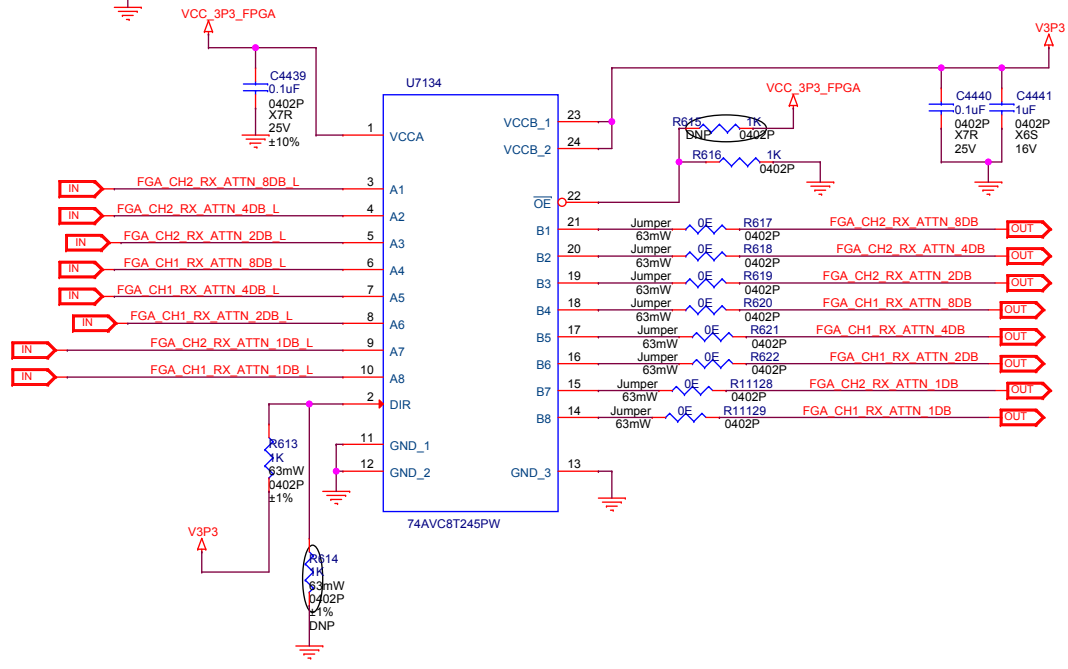
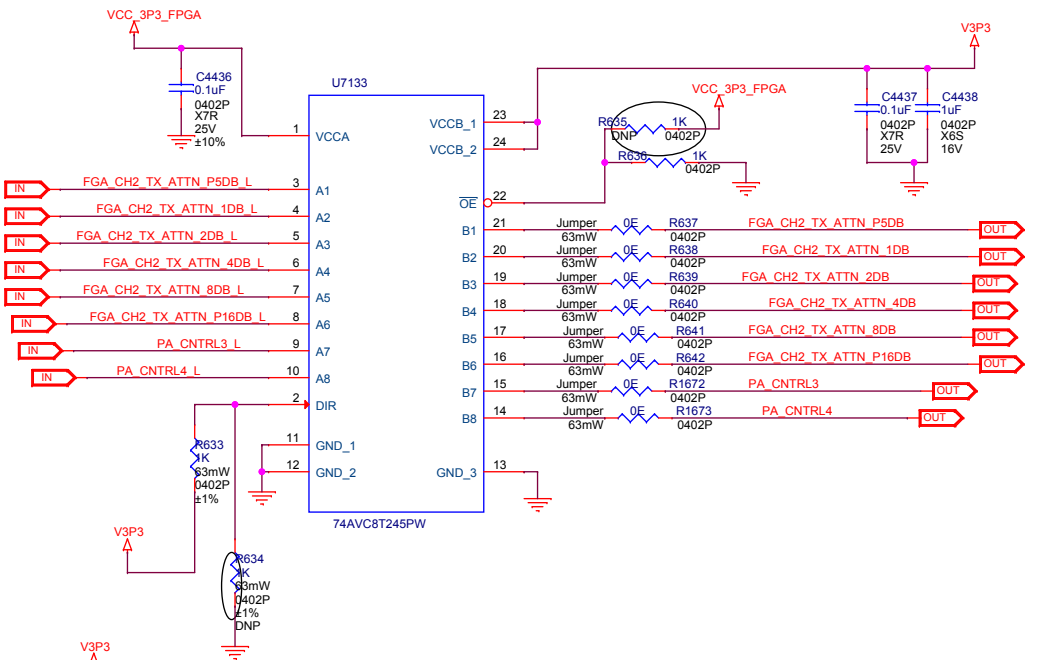
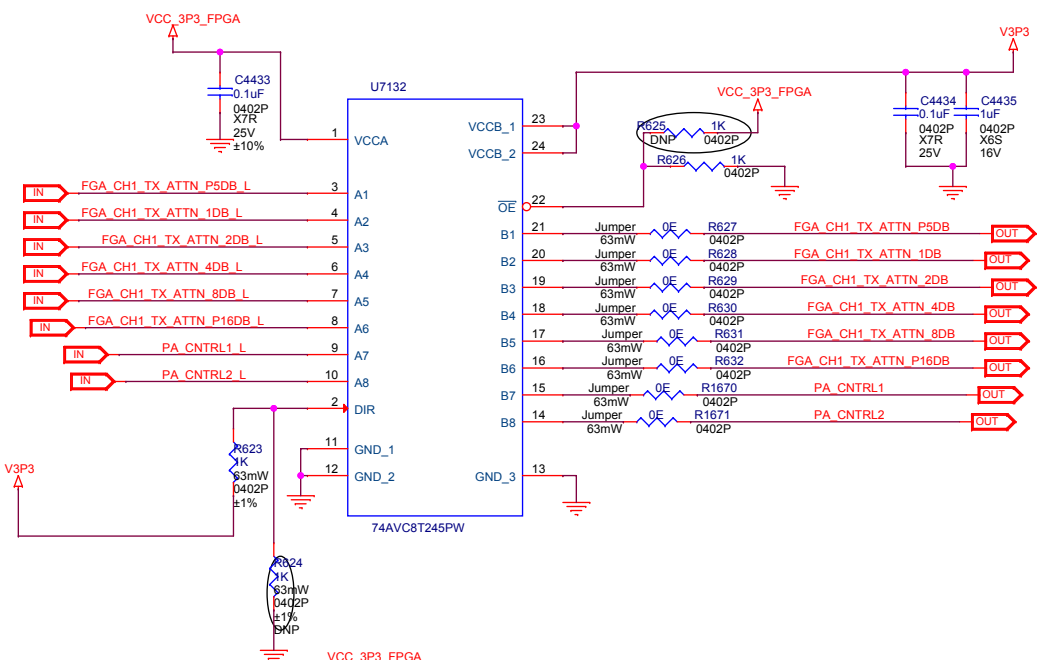
FPGA I2C BUFFERS



OpenCellular connect-1

Title		
FPGA_LVL_TRANSL_1		
Size	Document Number	Rev
A3		1.0
Date:	Thursday, December 01, 2016	Sheet 33 of 41

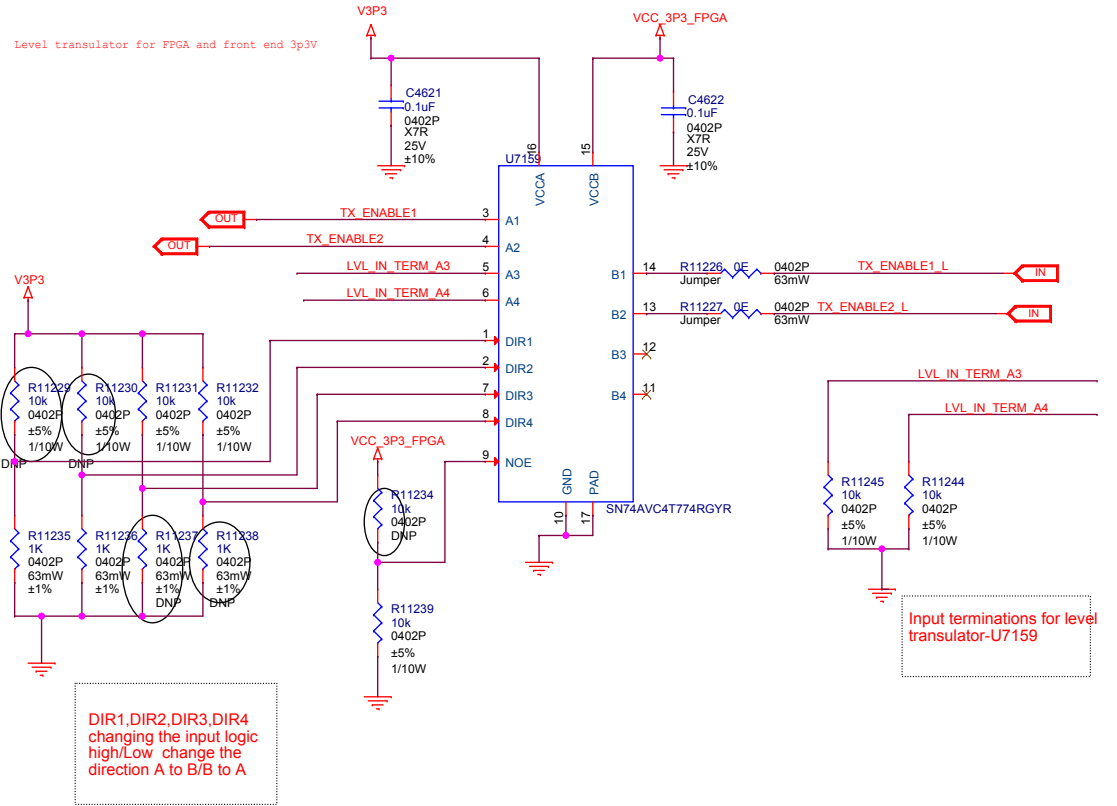
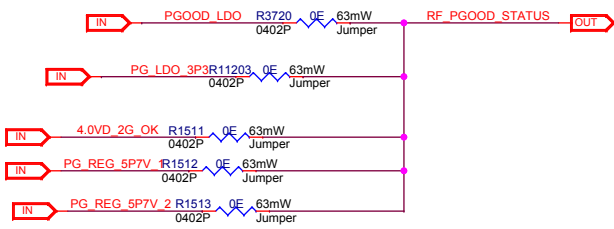
FPGA_RF_LVL_TRANSL



OpenCellular connect-1		
Title	FPGA_LVL_TRNSL_2	
Size	Document Number	Rev 1.0
Date:	Thursday, December 01, 2016	Sheet 34 of 41

TX ENABLE LVL TRNSL

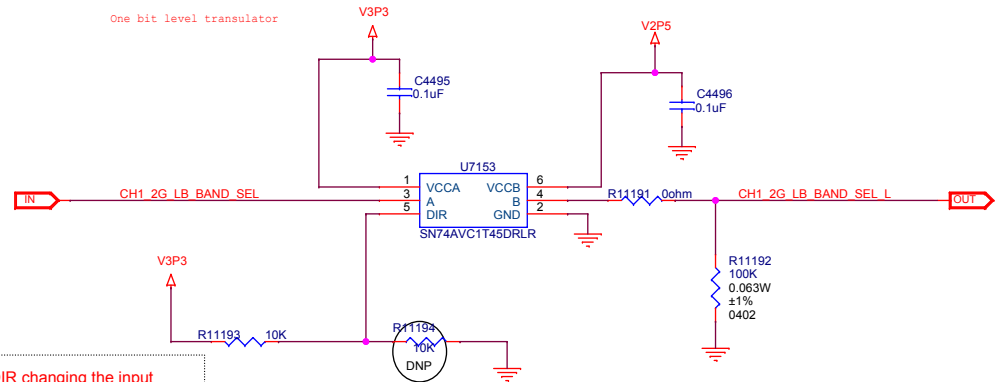
Comping all PGOOD status signals(open drain)



DIR1,DIR2,DIR3,DIR4
changing the input logic
high/Low change the
direction A to B/B to A

Input terminations for level
translator-U7159

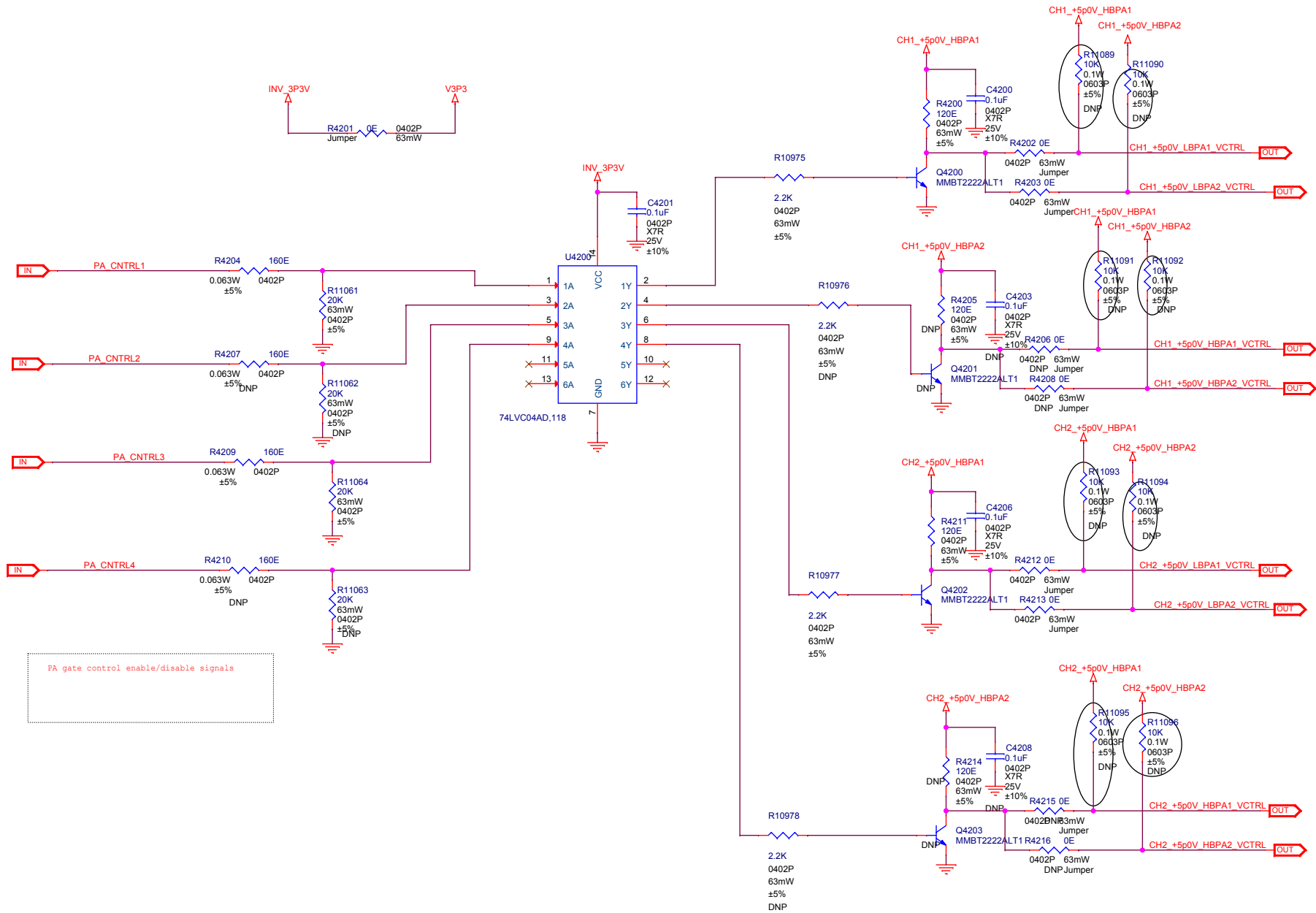
One bit level translator



DIR changing the input
logic high/Low change the
direction A to B/B to A

OpenCellular connect-1		
Title PGOOD_LVL_TRNSL		
Size A3	Document Number FBCON1RFSCSCH001	Rev 1.0
Date: Thursday, December 01, 2016	Sheet 35	of 41

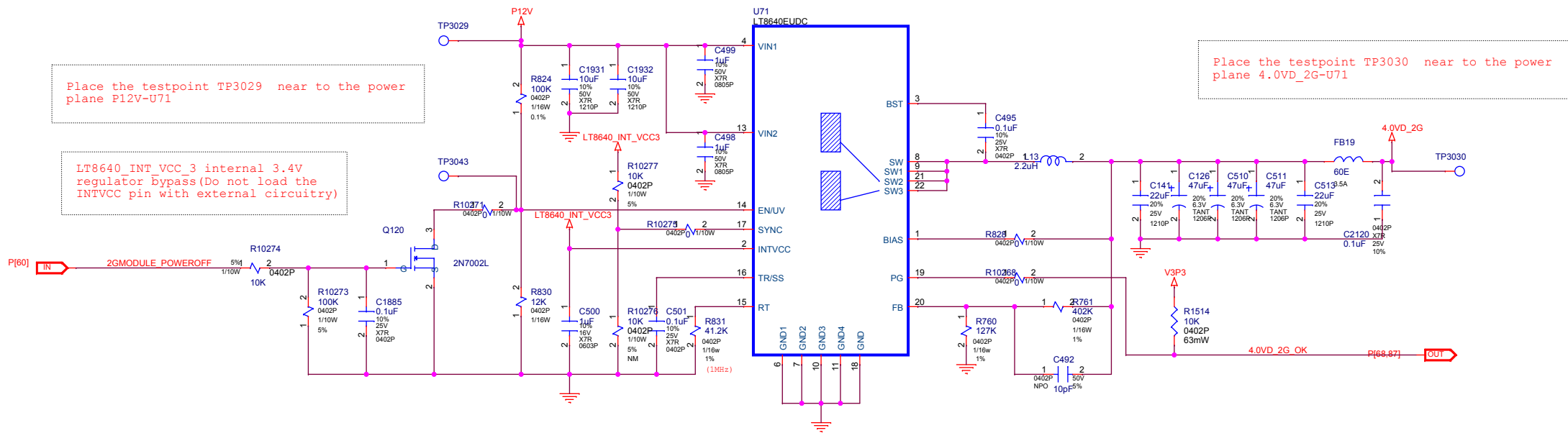
PA_ENABLE_CIRCUIT



PA gate control enable/disable signals

OpenCellular connect-1		
Title PA_ENABLES		
Size A3	Document Number	Rev 1.0
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12V_4V_2G_MODULE_POWER_SUPPLY

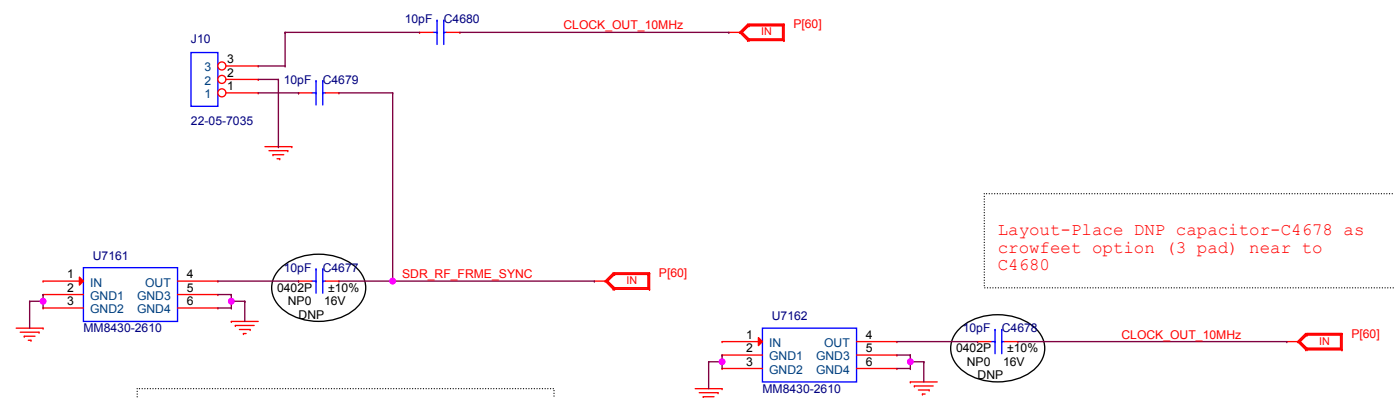


Place the testpoint TP3029 near to the power plane P12V-U71

LT8640_INT_VCC_3 internal 3.4V regulator Bypass (Do not load the INTVCC pin with external circuitry)

Place the testpoint TP3030 near to the power plane 4.0V_2G-U71

TEST CONNECTORS-10MHz, FRAM_SYNC

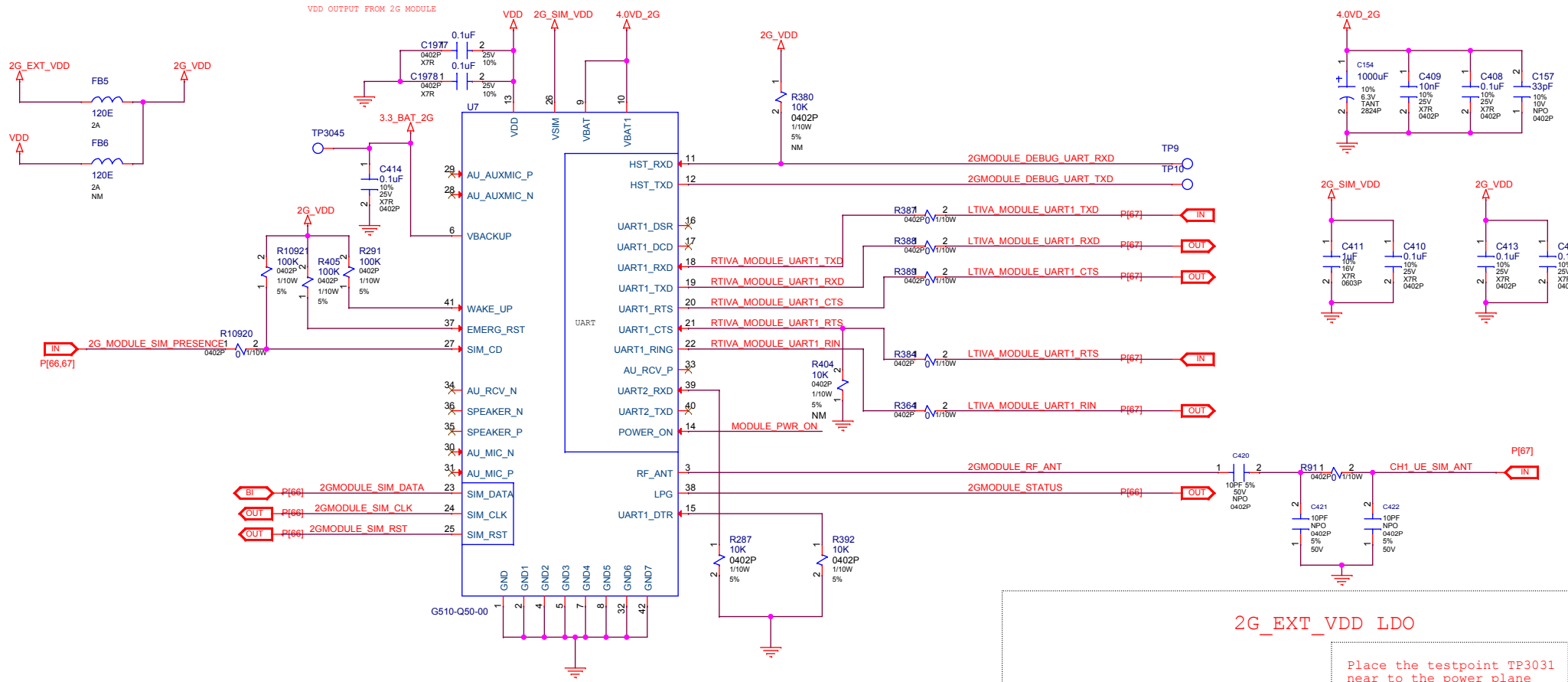


Layout-Place DNP capacitor-C4678 as crowfeet option (3 pad) near to C4680

Layout-Place DNP capacitor-C4677 as crowfeet option (3 pad) near to C4679

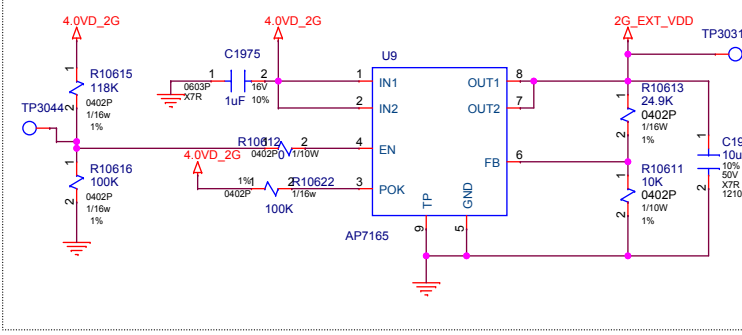
OpenCellular connect-1		
Title 12V_4V_REG_TEST_CONN		
Size A3	Document Number	Rev 1.0
Date: Thursday, December 01, 2016	Sheet 38	of 41

2G MODULE

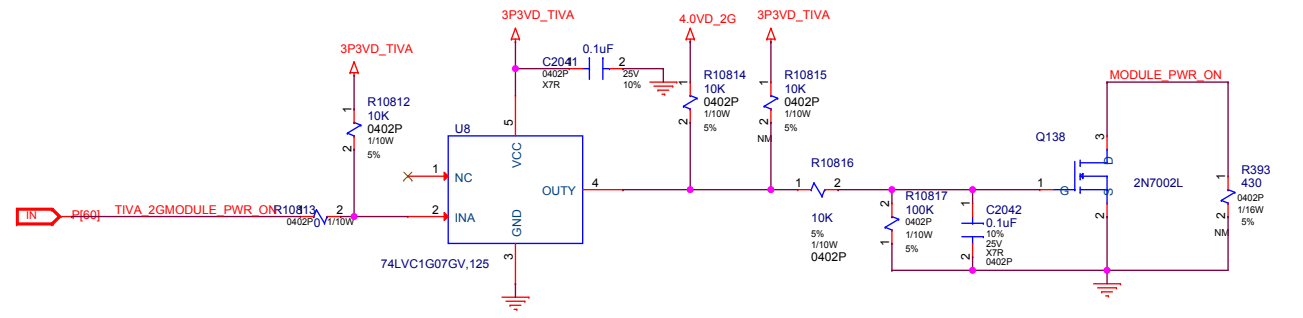


2G_EXT_VDD LDO

Place the testpoint TP3031 near to the power plane 2G_EXT_VDD-U9



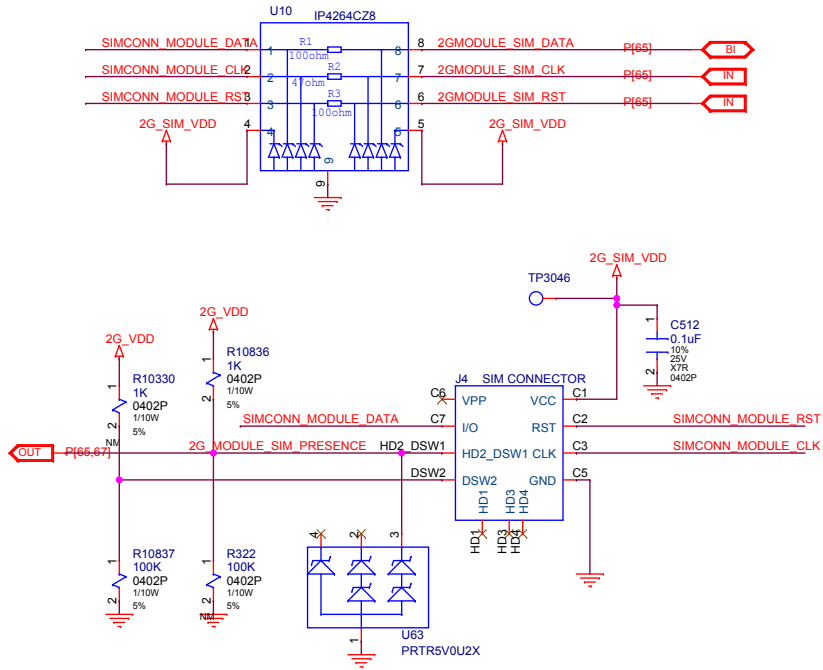
BUFFER WITH OPEN DRAIN OUTPUT



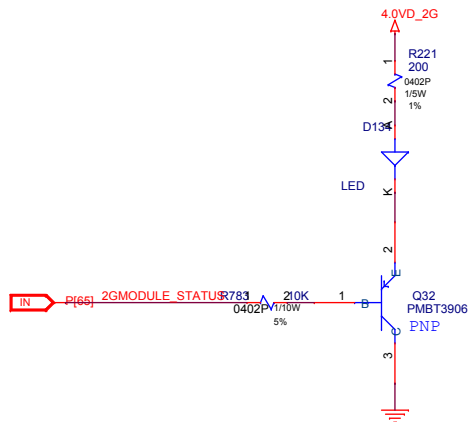
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Title	2G MODULE_1	
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2G MODULE 2

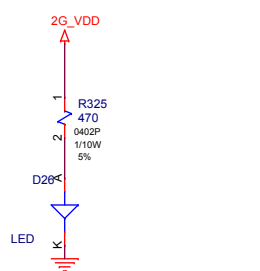
SIM CONNECTOR



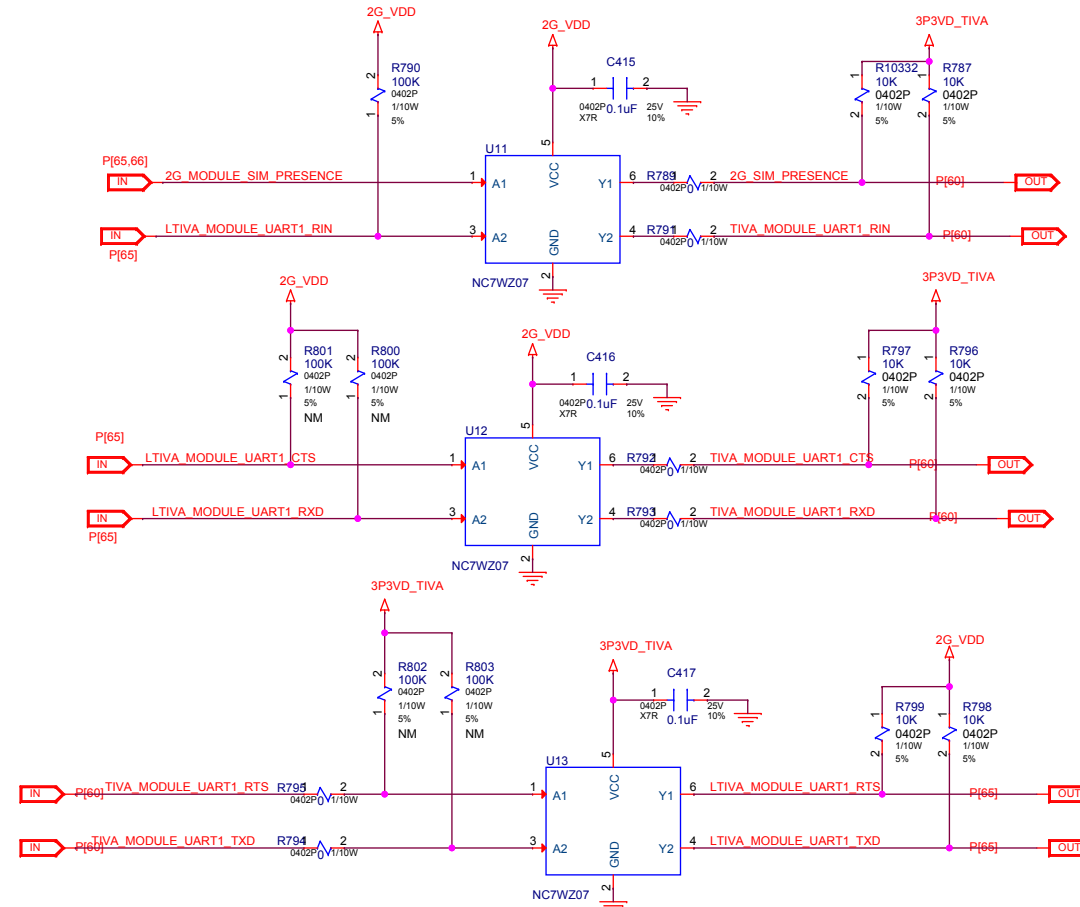
2G_MODULE STATUS LED INDICATION



2G_VDD LED INDICATION



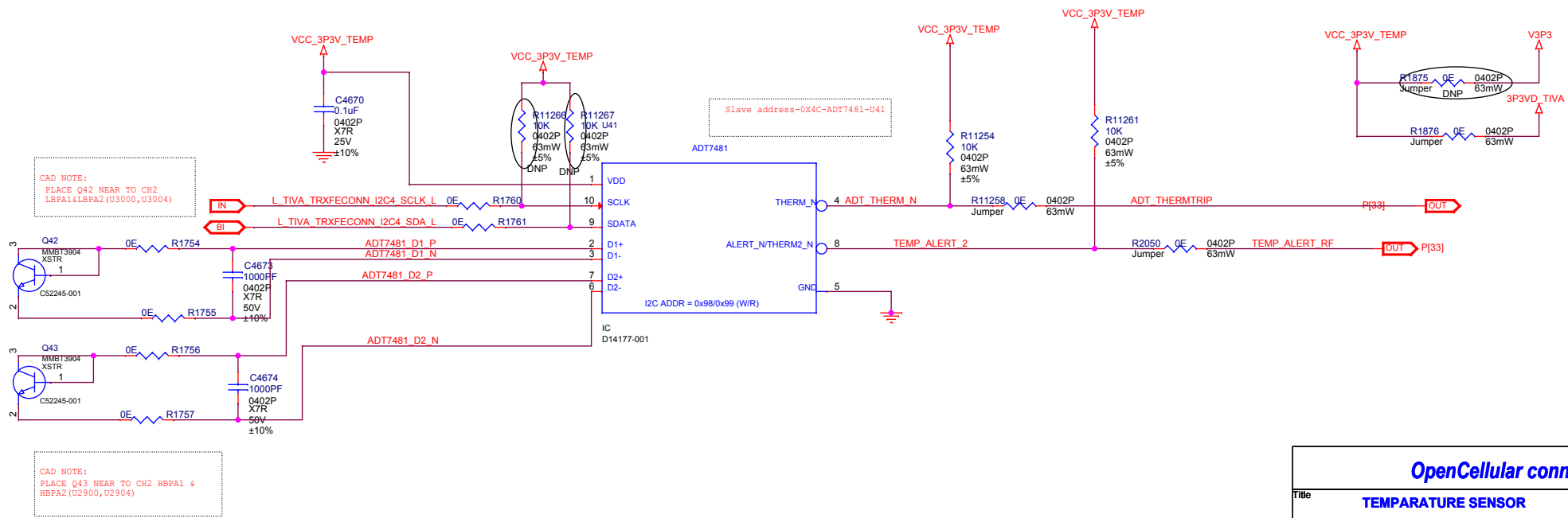
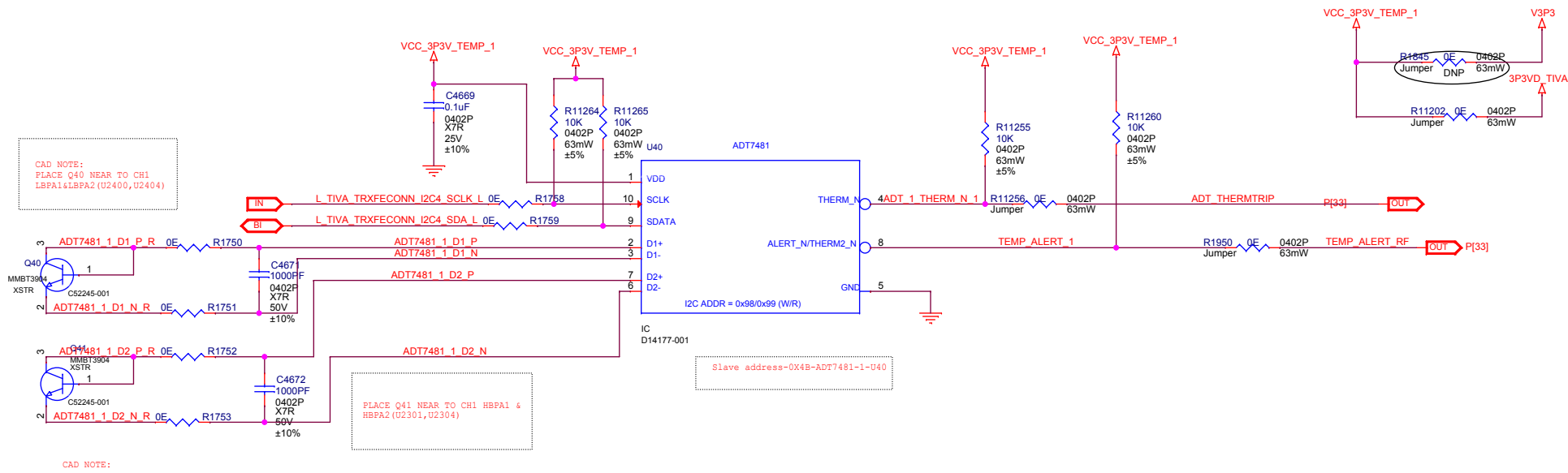
DUAL BUFFER



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TEMPERATURE SENSOR



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